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An investigation into the effects of power supply ripple on mixed signal devices and counter measures thereof

By

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The research work was carried out under supervision and direction of
Dr. Tom Conway
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Abstract

Precision instruments using mixed signal devices such as analog to digital converters (ADCs), digital to analog converters (DACs) and frequency synthesisers are sensitive to power supply noise and ripple associated with switch mode power supplies. The spectral composition of noise on a switch mode power supply output is examined. The question is posed as to whether precision mixed signal loads are sensitive to all power supply noise all of the time, or just some of the noise, some of the time The detailed nature of that sensitivity for each converter architecture is explored. Empirical power supply noise sensitivity data measured on a variety of ADC and DAC architectures, amplifiers and frequency synthesisers is presented. The performance degradation of these precision analog components resulting from the presence of power supply noise is shown. New data relating to the nature of a sigma-delta ADC's sensitivity to supply borne interference is presented. Passive low pass filters that adequately attenuate power supply noise incur a significant space penalty. Linear regulators used as power supply filters require a voltage drop that may be prohibitive. Two novel, different circuit techniques are proposed as solutions. Firstly, a completely novel technique whereby the power supply itself is subjected to a form of track and hold is proposed. That is to take account of the time-discontinuous nature of ADC sensitivity. The sinc function low pass filter characteristic of sampled and held waveforms is beneficially utilized as a power supply ripple filter. This technique is applied to both modified successive approximation and a sigma-delta ADCs. Two different ADC systems were redesigned to incorporate and test the necessary switch. Secondly, parallel resonance as a filter mechanism is proposed. The problems associated with using parallel resonance that have prevented its widespread adoption to date are covered and a novel auto tuning control circuit is presented in response. The automatic tuning circuit uses a specially fabricated barium strontium titanate (BST) variable capacitor as the tuning element. A phase comparison circuit is demonstrated as the control circuit. Results are presented from measurements taken powering a 16 bit pipelined ADC with and without the proposed filter. The volume required to accomplish the auto-tuned BST filter is compared to that achievable with a traditional LC low pass ripple blocking filter. An area saving of over 90% is shown. The unique suitability of this novel solution to full surface mount package encapsulation of the entire regulator and new filter is demonstrated. The work has yielded several patents.

Acknowledgements

I would like to express my sincere thanks to my supervisor Dr. Tom Conway for all his help, guidance, patience, support and advice.

In addition, the core research team of Aldrick Limjoco, Jefferson Eco, James Macasaet and Donal O Sullivan. Bill Hunt for his constant help in bringing me back to the fundamental principles. Adrian Sherry and Denis-A. Demspey for their specialist help on converter specifics. Shannon Yang for her specialist help on the control loop. Thanks to John Hassett at ADI for his financial support.

An anecdote from this journey.

I was lucky enough in life to work a little bit with the legendary Paul Brokaw in Analog Devices. Paul invented hundreds of the analog circuits we take for granted today and is a much decorated Fellow of the IEEE. He is a co-inventor with me of the patent outlined in section 5.4.2. As I contemplated the basic physics underlying this thesis and wondered how could parallel LC resonance actually be ? how does energy, i.e. mass, i.e. weight, transfer from an electric field to a magnetic field and back again ? I thought to ask Paul if he really understood parallel resonance. (One could get away with asking Paul such a question). His answer was interesting : "No. But I have some ideas ". So for those of you who think you have all this area fully mastered…..as Dr. Conway said "People who are too quick to answer generally didn't understand the complexity of the question"

Declaration

I hereby declare that the work detailed in this thesis is the result of my own investigations. No part of this work has been or is being submitted in candidature for any other degree.

Patrick J. Meehan

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Chapter 1 Introduction

1.1 Motivation and Background.

The author is a veteran of the analog semiconductor industry. Beginning his career as a SAR ADC designer, he went on to lead a team investigating the use on the fast Fourier transform (FFT) as a tool to analyse the dynamic performance of a sampling ADC. An outcome of that work was the author's discovery of how coherent sampling and a subsequently more accurate FFT result was physically implementable. This work was first published by him in 1987, [1], and has been widely cited. The author went on to work in the area of power supply management and contributed several, award-winning, completely new, product architectures and performance leading devices to the industry (Appendix A ADM1166). He has several patents granted from this period.

The observation that switch-mode power-supply noise is usually treated as broadband, always-destructive to accuracy and best remedied with physically large and expensive filters, that precision analog devices are usually not characterized but considered as sensitive to all types of power-supply noise all of the time led to the genesis of this project. The question as to whether power-supply noise is actually noise, per se, or is perhaps dominated by coherent and predictable signals is raised. Whether all analog and mixed-signal loads are sensitive to all power-supply noise all of the time or just some of the noise frequencies, some of the time is raised and answered. Then, with these answers, what better ways might exist to address switch-mode power supply output noise in a precision analog environment is explored.

1.2 Summary of Contributions

1. Full characterization and explanation of the sensitivity of a sigma-delta ADC to power-supply noise in this project is new. It has not been comprehensively done before, to the knowledge of the author or his peers.
2. Use of parallel resonance to filter power-supply noise in the way shown in this project is new.
3. Use of a barium strontium titanate variable capacitor as the tuning element in a power supply filter is new.
4. Use of a vertical lead-frame wall to isolate two surface mount inductors is new.
5. Use of a technique to temporarily reduce the parallel resonant filter Q factor, to enable tuning, is new.
6. Use of a track and hold as a filter on the actual power supply, while being powered from the device it is intended to filter is a totally new concept and architecture.
7. Four patents have been filed on the above list, by the author and his assistants. Two have been granted at the time of writing and two are pending.

   A paper has been published by Analog Devices, authored by two of the research team members who are Analog Devices employees, covering the true nature of ferrite beads. It was a sub-project (2.3.3) within this project and the author of this thesis is acknowledged as a technical contributor in that paper, [2]

1.3 Organisation of the Thesis

Chapter 2 begins with an overview of a generic power supply as used in a typical instrument that incorporates both digital (e.g. processor, memory) and analog functions (e.g. sensors, radios). The spectral content of a typical switched-mode power supply is examined and quantified. The components and settings that determine the spectral content of the switched-mode power supply output are discussed and conversely those that, to a first order, do not contribute to the spectral content, including the load, are examined.

The measured effect of the power supply interferers upon a typical, modern analog to digital converter is presented.

The circuit techniques in common use to attenuate power-supply noise and interference are examined and compared quantitatively based on the best performance claims found in the literature.

Chapter 3 presents a measurement technique used to quantify the sensitivity of analog to digital and digital to analog converters to power supply interferers. A representative example of each main architecture type of converter is measured and its sensitivity plotted. In the case of sigma-delta analog to digital converters, the thesis goes into detail to explain the different frequency regions of sensitivity and insensitivity.

Frequency devices such as phase-locked loop based frequency synthesisers are characterised for power supply sensitivity and the results presented. A typical modern operational amplifier is characterised and an explanation is offered on why it has the response as shown.

Having presented the problem in previous chapters, Chapter 4 introduces an entirely new solution to the problem of power supply ripple effecting analog to digital converters. It is hypothesised that a track and hold could be applied to the power supply of that section of the converter which is power-supply noise sensitive and powered from the insensitive section. The sinc function attenuation accompanying a track and hold function is then used to filter the supply ripple to the sensitive portion of the analog to digital converter. Theory, simulation and measured results of this hypothesis are presented.

Chapter 5 introduces a different solution. Parallel LC resonance is discussed as an option to filter power supply ripple. Its advantages and drawbacks are outlined. A barium strontium titanate dielectric variable capacitor is discussed as a tuning element in an automatic tuning circuit to be used in conjunction with parallel resonance. A circuit is built and tested with an ADC as load. Problems encountered with inductor to inductor coupling are outlined and a novel solution is shown. Enhancements to the tuning system in the event of multiple-frequency power-supply ripple content are presented and discussed. A lead frame assembly example of the suitability of this solution to full, single-package surface-mount integration was built and is shown.

1.4 Acronyms and Symbols

AC	-	Alternating Current
AC PSRR	-	Power Supply Rejection Ratio measured with an AC test tone
ADC	-	Analog to Digital Converter
ADICE	-	Analog Device Integrated Circuit Emulator
AVDD	-	Positive Power Supply to Analog Circuitry
BiCMOS	-	Fabrication process combining CMOS and bipolar
BST	-	Barium Strontium Titanate
C	-	Capacitance
CCM	-	Continuous Conduction Mode
Cmax	-	Maximum Capacitance
Cmin	-	Minimum Capacitance
CMOS	-	Complimentary Metal Oxide Semiconductor
Cos	-	Cosine
D	-	Duty Cycle
dB	-	Decibels
dBc	-	Decibels Relative to the Carrier
dBFS	-	Decibels Relative to Full Scale
dBm	-	Decibels Relative to 1 mW
DC	-	Direct Current
DC/DC	-	DC to DC converter/regulator
DCR	-	DC resistance
deg.	-	Degrees
DVDD	-	Positive Power Supply to Digital Circuitry
ENOB	-	Effective Number of Bits
FFT	-	Fast Fourier Transform
Fmod	-	Modulator Frequency
Fs	-	Sampling Frequency
Fsw	-	Switching Frequency
GM	-	Transconductance Amplifier
Gnd	-	Ground
GSPS	-	Giga Samples Per Second
Hz	-	Hertz
IOVDD	-	Positive Power Supply to IO Circuitry
L	-	Inductance
LPF	-	Low Pass Filter
LSB	-	Least Significant Bit
MCLK	-	Master Clock

ms	-	Milliseconds
MSB	-	Most Significant Bit
MSPS	-	Mega Samples Per Second
mV	-	Millivolts
PFM	-	Pulse Frequency Modulation
PLL	-	Phase Locked Loop
PSRR	-	Power Supply Rejection Ratio
PWM	-	Pulse Width Modulation
Q	-	Quality Factor (Z/R)
R-2R	-	A resistor ladder comprising R and 2 R branches
RF	-	Radio Frequency
RMS	-	Root Mean Square
SAR	-	Successive Approximation Register
Simplis	-	A software simulation product
Sin	-	Sine
Sinc	-	Cardinal Sine Function
Sync/Err	-	Synchronized or Error Signal
V	-	Volts
VCO	-	Voltage Controlled Oscillator
Vdd	-	Positive Power Supply
Vin	-	Input Voltage
Vout	-	Output Voltage
Vref	-	Reference Voltage
Vss	-	Negative power supply
WCDMA	-	Wideband Code Division Multiple Access
wt	-	Omega t. ($2\pi ft$)
Φ	-	Theta (Phase Angle)
Ω	-	Ohm

Chapter 2 Spectral content of power-supply noise.

The main aim of this chapter is to discuss the frequency content produced by the power supply topologies that are most commonly used to power mixed-signal loads. Measures such as efficiency, line and load regulation are already well known for these power supply choices. It is the frequency and relative energy content of the unwanted interferers seen on the power supplies' outputs that is focussed on here. The conventional techniques of low-pass filtering, post regulation, ferrite beads and alternative architectures are considered and their limitations discussed.

This chapter lays the foundation for Chapter 3 where the sensitivity of various mixed-signal loads to the spectral profiles seen in this chapter will be discussed.

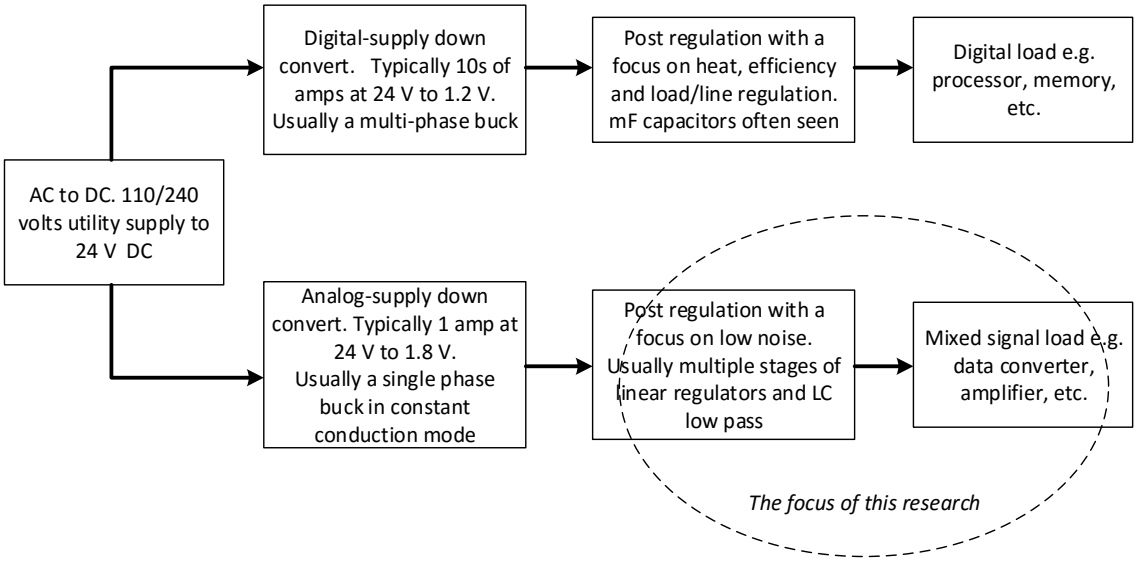


Figure 2-1 A generic system power supply.

A simplified block diagram of a generic power supply flow for any typical system with separate digital and mixed signal elements is shown in Figure 2-1. Digital and mixed-

signal loads have different requirements in terms of noise and power. For this reason they are generated as separate power supplies with different emphasis. However, the trend is for digital power rails to face similar requirements to mixed-signal rail, driven by lower voltages and higher signal speeds.

2.1.1 **Power supplies for digital loads.**

The need for higher speed, more integration and lower cost has caused consequent, ever-shrinking semiconductor process geometries which, in turn, drive gate voltages down to the less than 1 V and currents up to several tens of amps to maintain even the same power as earlier generations. Switching speeds in GHz drawing tens of amps require a digital power supply that can stay in line and load regulation despite the demands of the digital load as gates switch drawing transient currents. Increased drive for energy efficiency and battery lifetime overlays a requirement that the power supply performs in as efficient a manner as possible. Digital power supplies use techniques such as multi-phase switching regulators and digital power factor correction to achieve this. The focus in this area of power supply design today is on system reliability metrics, power-supply sequencing management, brown-out recording and power factor correction [3] [4].

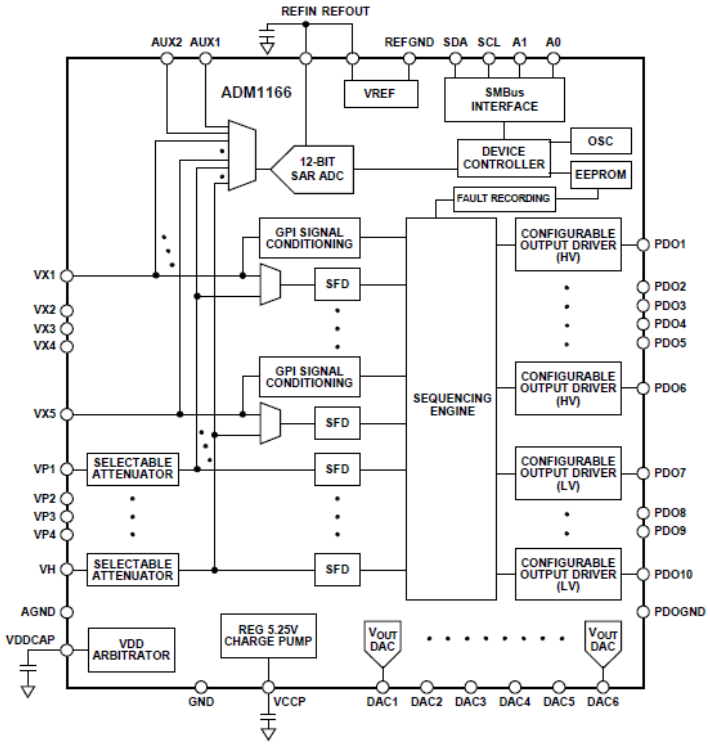


Figure 2-2 A post-regulation digital power supply manager [3]

An example state of the art device designed for use in power supplies intended to power digital loads is shown in Figure 2-2. It is included here to show where digital power rail research is currently focussed. The purpose of this device is to allow programmable control of the on / off sequence of the various rails and to monitor their voltages. A non-volatile record is kept of the most recent voltage status of the rails monitored. The data sheet for this device (ADM1166) is included in Appendix A ADM1166. (Its definition was a direct output of the early stages of the research carried out for this thesis.)

2.1.2 **Power supplies for analog / mixed-signal loads**

The key performance specification on apparatus used in analog applications ranging from medical, to avionics to industrial process-control will come down to the reliably achievable performance of the analog section. Analog loads such as amplifiers, data

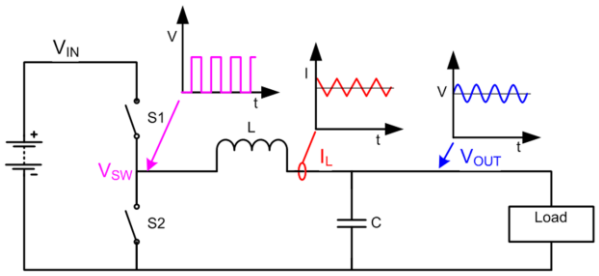
converters and frequency management devices are specified for ever increasing precision, resolution and speed in a constantly reduced area. The business requirement to achieve ever faster times to market for ever more complex analog multifunction devices has forced system power supply designers to adopt an auxiliary or redundancy system strategy to designing the power supply rails intended to power these loads. Without knowing the exact sensitivity of the analog load to power supply borne interferers, the system designer typically relies on linear regulators followed by π-configuration, multi stage LC low-pass, ferrite beads and decoupling capacitors [5].

The intermediate rails available will typically be 12 V for PC based systems, 24 V for industrial and 48 V for telecommunications. Dropping to the typical analog rail of 1.8 V at 1 A and greater involves too much power wastage for linear regulation to be commonly used for anything other than post-regulation filtering. A switching regulator designed to operate as a continuous conduction mode (CCM) buck is commonly used as the primary down converter from the intermediate rail to the near-final voltage. Discontinuous conduction is unpopular as the on / off pattern suggests unpredictable interferers emanating from that block. Within the CCM range, Pulse Frequency Mode (PFM) also known as Power Save Mode is used to save power at light loads. It is less popular than Pulse Width Modulation (PWM) when powering high performance mixed-signal loads because it is undesirable to vary the interference frequency to a mixed-signal load in a non-predetermined manner [6]. The balance of this section will now focus on the spectral content seen at the output of a typical buck regulator used in PWM CCM mode and how it applies to mixed-signal loads.

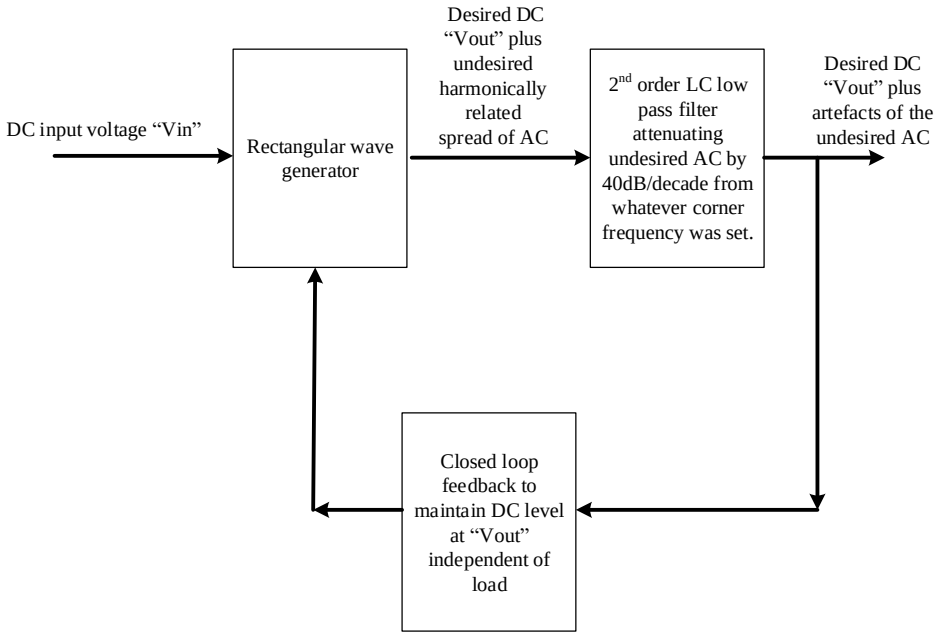
2.2 Spectral content of a switching regulator operated in PWM buck CCM.

2.2.1 Introduction

Switching regulators are conventionally described in the time domain as a number of phases of charging and discharging inductors and capacitors where peak currents and voltages are the primary focus, [7]. But for the purpose of this research it is useful to view them in the frequency domain instead, where spectral content is of greatest interest.



(A)



(B)

Figure 2-3 (A) Time domain and (B) Frequency domain representation of a switching regulator.

Figure 2-3 shows circuit and block diagram representations of a switching regulator of the type described. The purpose of the switches is to generate a rectangular waveform with a DC average that equates to the desired final DC output. For example, in the case of a Vout = 0.5 Vin arrangement, a 50% duty cycle square wave will result. Its DC value is half Vin.

The storage inductor and capacitor form a second order LC low-pass filter. Its purpose is to filter all the AC content, called "ripple", and leave just the DC average. The

larger the LC product, the lower the corner frequency and the more attenuation is applied to the AC content which has its fundamental component at the switching frequency and harmonics thereafter. Switching regulator design is essentially a trade-off between having the LC corner frequency low enough to remove enough of the AC content balanced against keeping the physical L and C size within useful bounds [7].

$$Vripple(pp) = (V_{in} - V_{out})D/(8f_{sw}^2LC) \qquad \text{Equation 1}$$

Equation 1 gives the peak to peak ripple seen on the output of an ideal buck, CCM, PWM switching regulator [7]. The denominator term suggests that in the case of ideal components, making the corner frequency of the LC filter, $F_c = 1/2\pi\sqrt{(LC)}$, as low as possible relative to the switching frequency (Fsw) are the only parameters that allow the ripple to the adjusted for a given Vin to Vout / duty cycle ratio.

Further, the regulator has a closed loop which attempts to keep the DC output at a pre-set level. The LC filter acts against the speed of this loop as the filter corner frequency drops. Thus the line and load response of the regulator is adversely affected by the increased filter size.

2.2.2 **Variation range of harmonic level within regulation range.**

The periodic waveform produced by the switches in the switching regulator have a harmonic content related to duty cycle, switching frequency and input amplitude [8]. The level of each individual harmonic is given by Equation 2.

$$Vk = 2Vin\left(\frac{Sin(\pi kD)}{\pi k}\right) \qquad \text{Equation 2}$$

Where k = Harmonic number, D = Duty cycle (on time as a fraction of total time).

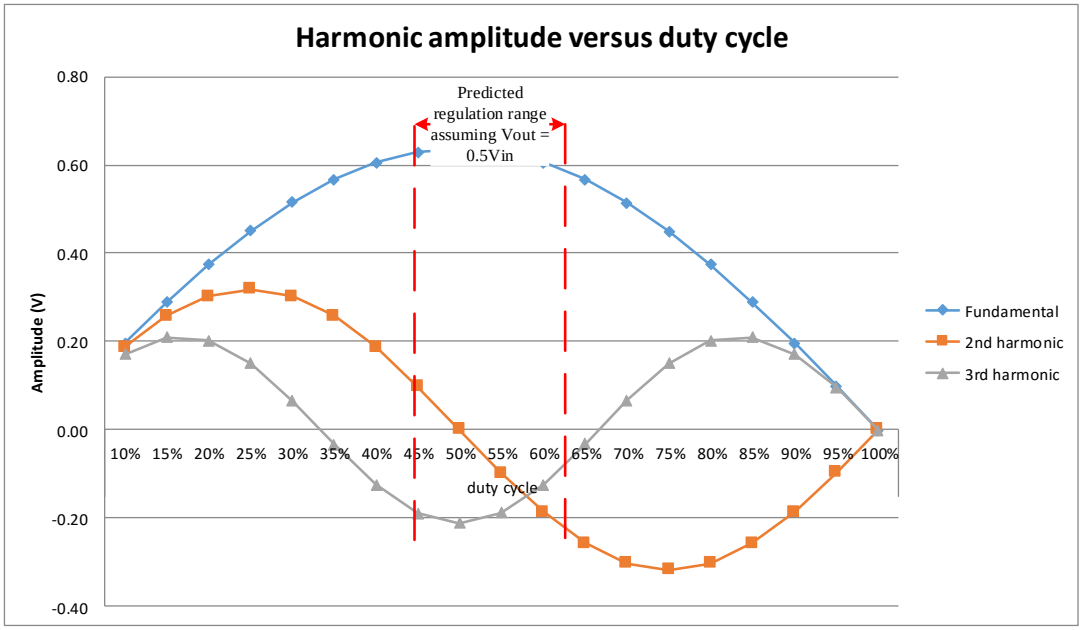
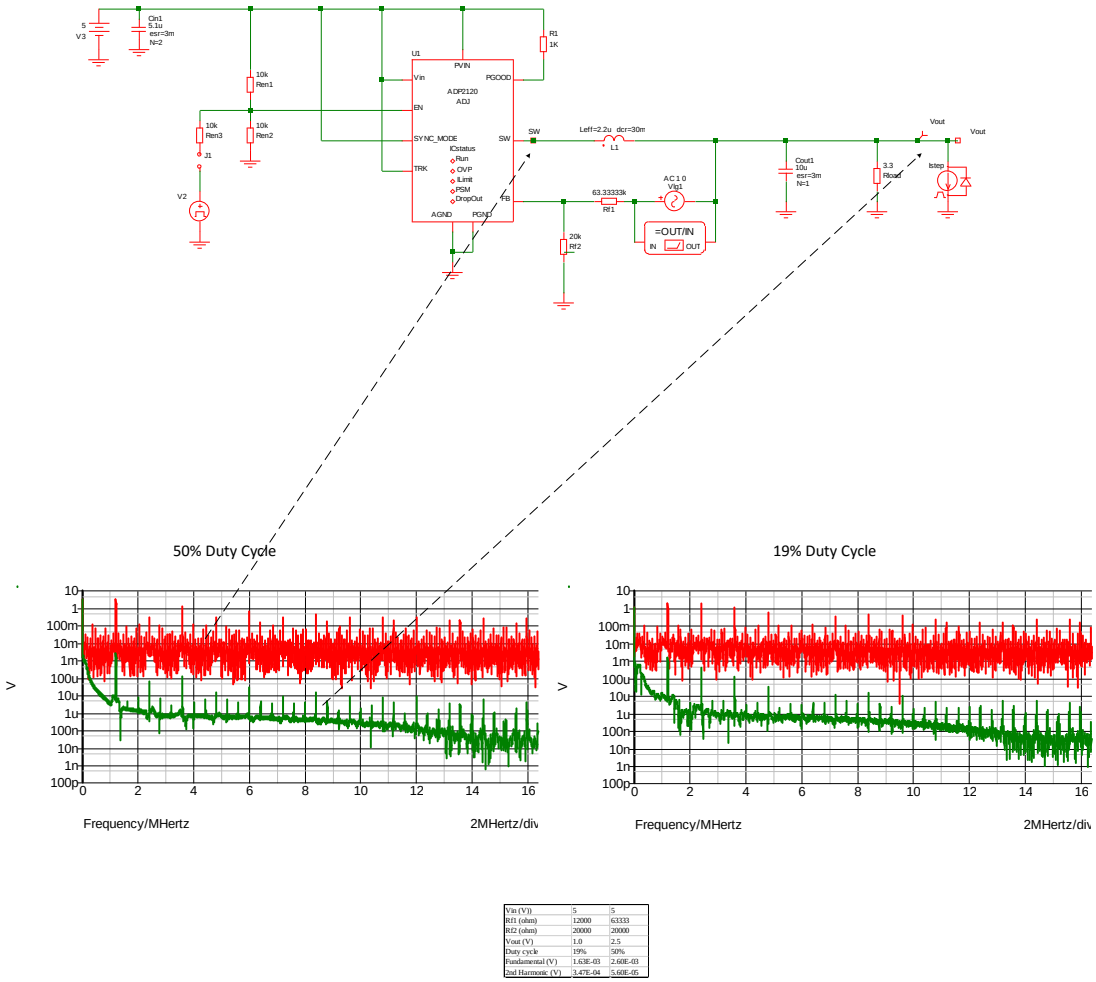


Figure 2-4 Harmonic amplitude versus regulator duty cycle

Figure 2-4 Uses Equation 2 to plot the amplitude of the fundamental, the second and the third harmonics for the case of an ideal switching regulator with a 1 V input, before the attenuation of the storage inductor and capacitor are taken into account as covered in [8]. The hypothetical case where the PWM regulation ranges from 40% to 60% as the regulator loop attempts to keep Vout constant at 50% of Vin, as the load varies is shown by dotted red lines. This thesis presents a focus on that case only. It does not discuss cases outside of that range, where the second harmonic could be relatively larger or regulator architectures which could give rise to significant sub-harmonic content. The fundamental magnitude ranges from 0.61 V to 0.64 V but the second harmonic ranges from 0.19 V at 40%, through zero at 50% to -0.19 V at 60%. Thus the second harmonic will see far more variation than the fundamental from the effect

of the regulation loop action at near 2:1 divide ratios of the input voltage as an example scenario.

To calculate the level of each individual harmonic at the switching regulator output, after the LC filter, one simply applies a 40dB/Decade roll off to the level given by Equation 2.



Vin (V))	5	5
Rf1 (ohm)	12000	63333
Rf2 (ohm)	20000	20000
Vout (V)	1.0	2.5
Duty cycle	19%	50%
Fundamental (V)	1.63E-03	2.60E-03
2nd Harmonic (V)	3.47E-04	5.60E-05

Figure 2-5 Simulation run on an ADP2120 switching regulator

A simulation run on an ADP2120 switching regulator operating at 1.5 MHz is shown in Figure 2-5. A SIMPLIS [9] model was used and the Fourier probe utility used to

probe the switch and output nodes in both 19% and 50% duty cycle conditions. The difference between the red and green traces shows the low pass effect of the 2.2 μH and 10 μF storage inductor and capacitor values chosen. This combination gives a corner frequency of 33 kHz. Equation 2 can be used to calculate the fundamental and harmonic magnitudes at the switch node and apply a 40dB / decade attenuation to them from the LC filter. There is correlation with the simulation results to better than 1%. Therefore, with just knowledge of the voltage divide ratio, the switching frequency, the filter component values and the AC-PSRRload sensitivity, it is possible to accurately calculate the power supply interference level at specific harmonic frequencies that a load will see.

2.2.3 **The effect on a mixed-signal load of the harmonic content from a switching regulator supply.**

The question as to the importance to a mixed-signal load of the spectral content on the output of the switching regulator intended to down convert the upstream power supply rail is dealt with in detail in Chapter 3. However, an introduction is given here so that the subsequent discussion in the remainder of this chapter is contextualized.

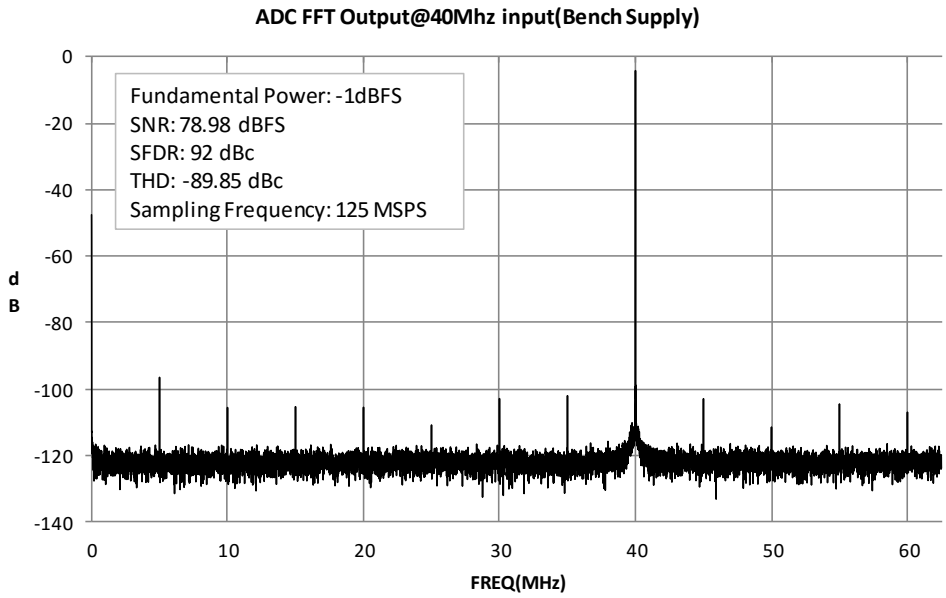


Figure 2-6 FFT of a AD9268 16-bit pipelined 125 MHz ADC digitizing a 40 MHz signal with a linear power supply.

Figure 2-6 shows the FFT taken from the measured output of a modern 16 bit pipelined analog to digital converter (ADC) digitizing a 40 MHz coherently sampled test-signal. Coherent sampling means that an integer number of salmples were digitized, [1] The power supply was a clean, linear 1.8 V laboratory unit. The reference was the internal 1 V reference on the ADC die. The various harmonics and spurs seen above the quantization floor at -120 dB to full scale are artefacts resulting from the ADC's non-linearity [10], [11]. The spurious-free dynamic (SFDR) range achieved is the manufacturer's specified 92dB.

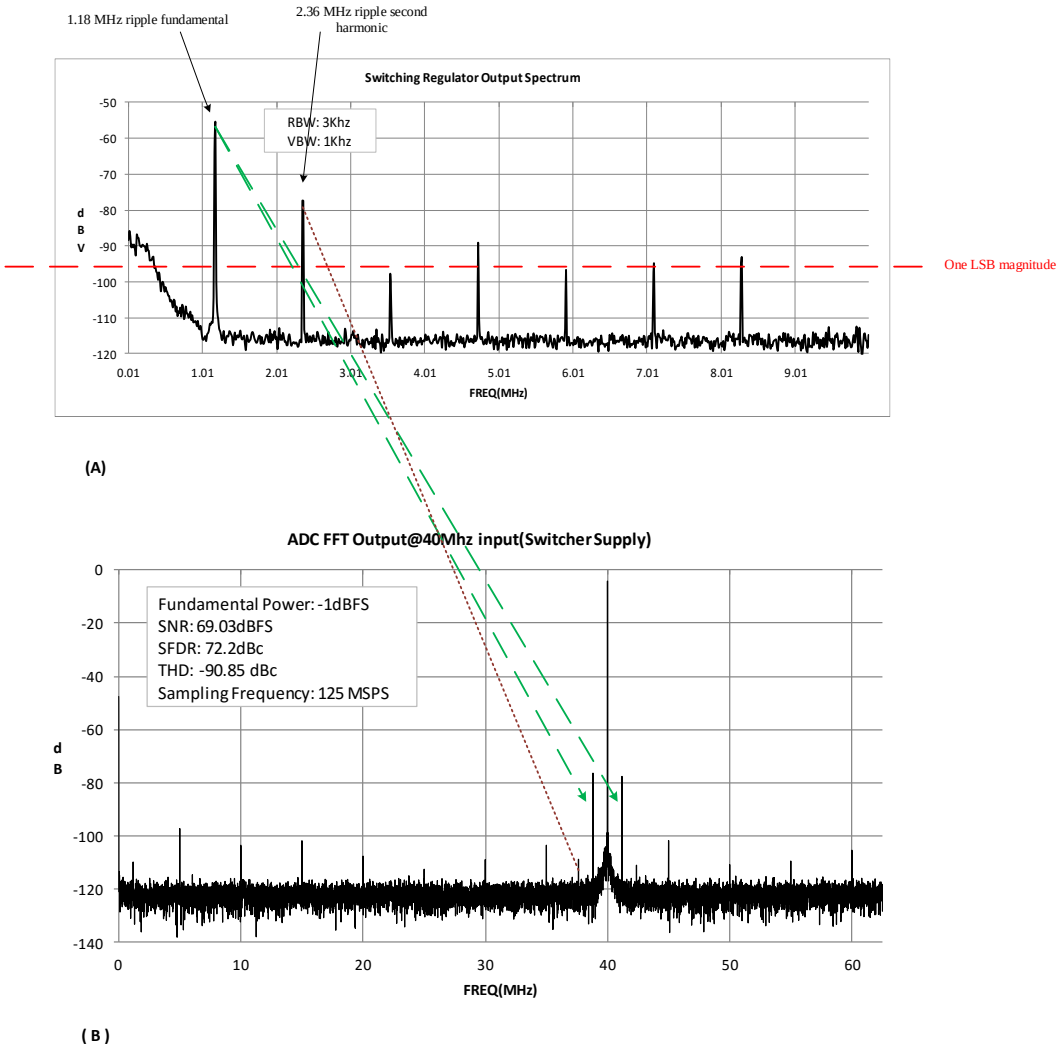


Figure 2-7 The effect on an AD9268 16 bit pipelined ADC of switching regulator ripple on its power supply. The regulator output in (A) and the ADC output in (B).

The same ADC used in Figure 2-6 is now powered from a switching regulator. The spectra are shown in Figure 2-7. The 0.1 µF decoupling capacitor remained in place at the ADC. The top plot in Figure 2-7 shows the measured spectral content of the switching regulator as described in section 2.2.2 The dotted horizontal red line is drawn at -96 dBV which is the size of one 16 bit LSB for the one volt internal reference used. In this example the switching frequency fundamental ripple of 1.18 MHz intermodulates with the 40 MHz input signal to produce sum and difference

frequencies. However, in this specific case the fundamental ripple frequency does not appear above the quantization noise floor in the ADC output spectrum at its fundamental location. It is only seen as an intermodulation term. The net result is that the spurious-free dynamic range is reduced from 92 dB to 72 dB by the presence of the fundamental frequency component of the switching regulator ripple. An adverse effect of 20dB or 3 bits of effective resolution is lost from this 16 bit ADC in the presence of the fundamental switching regulator ripple, even with decoupling present. Decoupling is of a finite value, related to its reactance at the interference frequency, its parasitic R,L,C values and its distance from the load.

2.3 Techniques available to reduce power supply output ripple.

There are many known techniques available to reduce power supply output ripple. In the context of Figure 2-3, this may be viewed as attempts to improve the order of the existing filter that the switching regulator is constructed from. It is to be noted here that an active filter is not considered as the extra power supply for the amplifiers would not be available, except in the case of a linear regulator which is powered from the rail to be filtered. This section will now briefly outline the more common choices and outline their drawbacks.

2.3.1 **Multiphase regulation**

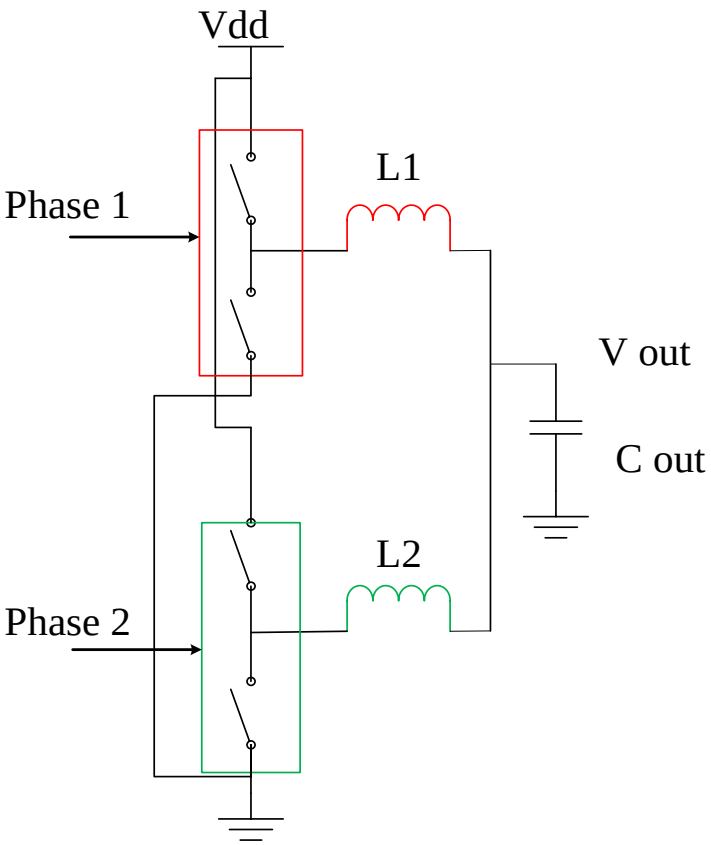


Figure 2-8 Basic two-phase buck regulator

A basic two-phase implementation of a multi-phase buck regulator is shown in Figure 2-8. Multiphase regulation is commonly used in higher power systems (> 25 amps) [12] to effectively reduce the RMS current seen by each switch by a factor N, the number of phases. This reduces heat dissipation and hot spots on the power supply board. However, use of multiple phases also reduces power supply ripple by a factor dependent on the number of phases, N, and the duty cycle, D.

Equation 3 gives the normalized percentage of ripple cancelled relative to a single phase buck [12].

$$Irip_{norm} = N * \frac{[D - mp(D)]}{N} * \left[\frac{1 + mp(D)}{N} - D\right] / [(1 - D)D\ ] \qquad \text{Equation 3}$$

Figure 2-9 shows a plot of calculated normalized ripple for the different cases of a two phase and a twenty phase buck regulators. The hypothetical situation of a duty cycle variation between 40% and 60% is taken as representative of the span over which the regulation loop might sweep as the regulator keeps the output in regulation. This is indicated by two vertical red dotted lines in the diagram. This duty cycle variation results in a maximum normalized ripple shown as a green dotted horizontal line of 33% occurring at 0.4 duty cycle for a two-phase and 4.9% occurring at 0.42 duty cycle for a twenty-phase. In more familiar filter metrics, this is a 9.6 dB ripple attenuation from use of a two-phase and 26.2 dB ripple attenuation from use of twenty phases, all given a boundary condition of a 20% necessary duty cycle variation. In later chapters this will be compared to that achieved by a novel ripple filtration technique.

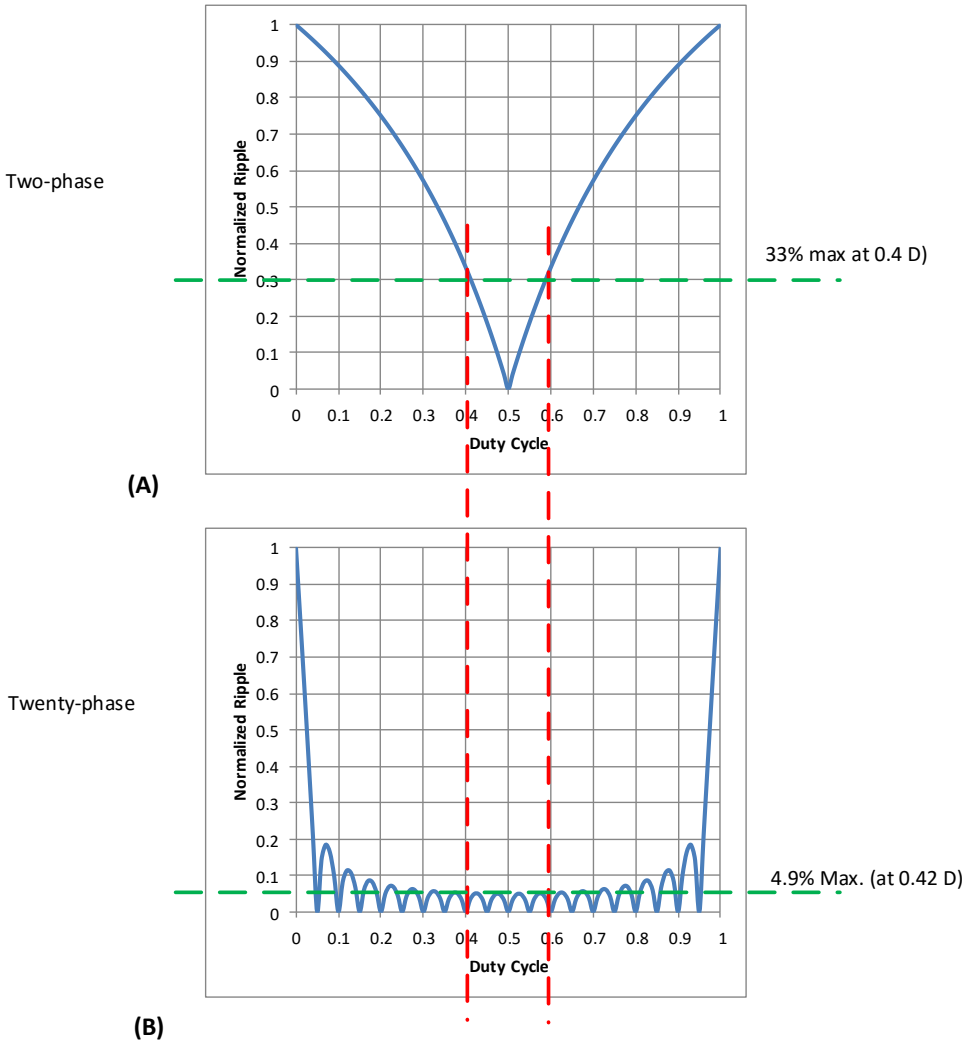


Figure 2-9 Normalized ripple comparison for example two (A) and twenty phase (B) buck regulators

2.3.2 **Linear regulation**

Linear regulators are commonly used after the switching regulator to reduce both broadband noise and power supply ripple. A linear regulator's ability to attenuate ripple is characterized by its AC power supply rejection specification (AC PSRR). It is a measure of the output amplifier bandwidth of the linear regulator, i.e. how quickly the amplifier can cause a loop response to cancel out the AC seen on the power supply. Figure 2-10 shows the AC PSRR plot from a leading linear regulator at the time of

writing [13]. It was designed as a direct outcome of this research and specifically defined to maximize its ability to attenuate switching regulator ripple. The data sheet for this device is included in Appendix B,(ADM7150). Other aspects such as size, cost, fabrication process and supply current were traded in favour of maximizing AC PSRR. The first pole in the amplifier response occurs at approximately 60 kHz and falls at a double pole rate from 100 dB rejection at 60 kHz to 60dB rejection at 1 MHz. These measurements were taken with a 6.2 V input and a 5 V output, i.e. a 1.2 volt support voltage was used to achieve this level of ripple rejection.

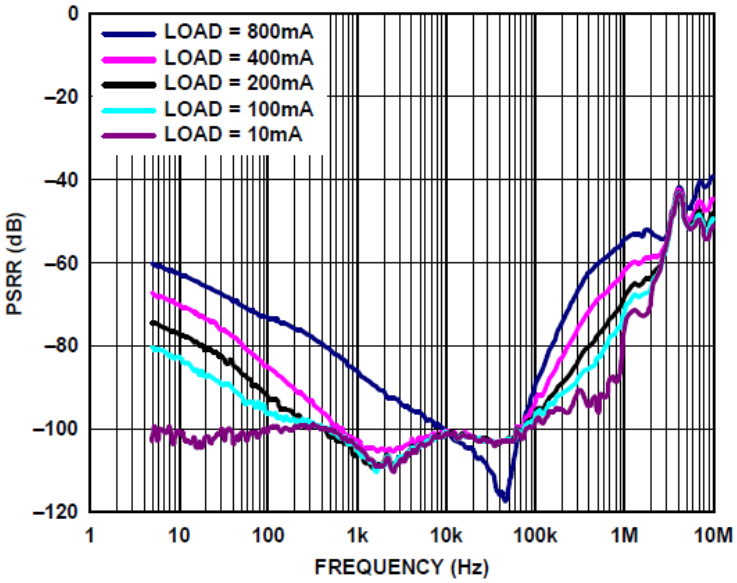


Figure 2-10 AC PSRR of a state of the art linear regulator [13]

2.3.3 **Ferrite beads.**

Ferrite beads are composed of a bead of ferrite ceramic encapsulating a conductor. Their principle of operation is that the AC related magnetic field energy is dissipated as heat in the ferrite material whilst DC passes through the conductor unaffected.

Their use in power supply circuits is practically ubiquitous even though they are designed to be used as attenuators in the hundreds of MHz region. Many designers consider them as a catch-all filter operating across the AC spectrum. In reality, ferrite beads have little or no attenuation at typical switching regulator ripple frequencies. Instead they do offer a substantial risk of series resonance at the frequencies involved and a consequent potential for voltage magnification rather than attenuation.

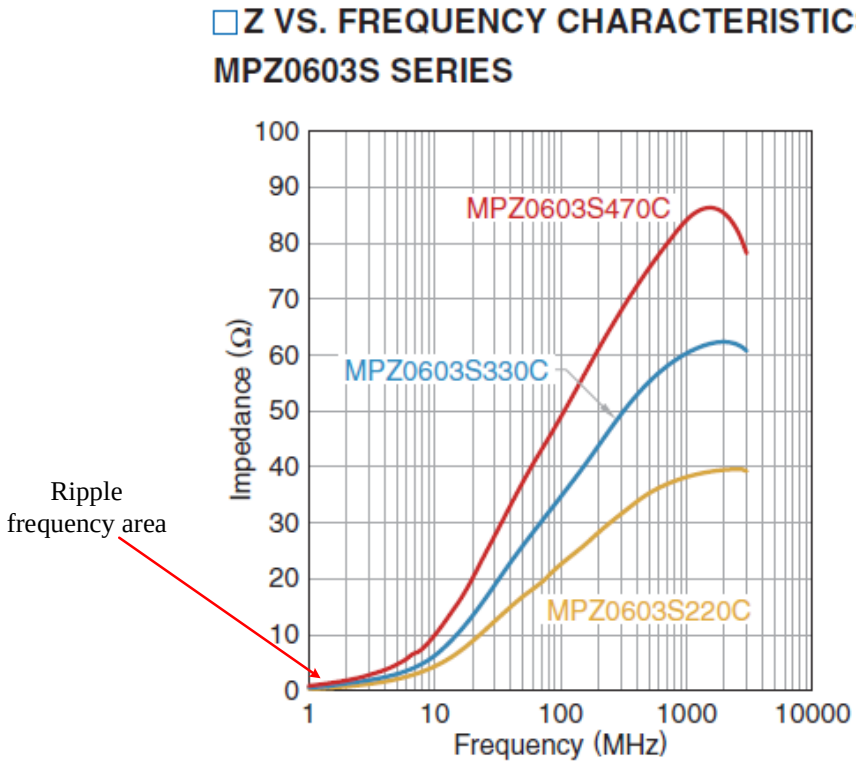


Figure 2-11 Impedance versus frequency for typical ferrite bead filters [14].

Figure 2-11 shows the typical performance curves of the TDK MPZ series of ferrite beads as an example of a popular bead choice. Whilst ferrite beads do offer useful attenuation at the overshoot and undershoot frequencies for which they are intended, they offer little attenuation at the fundamental and near harmonics of the ripple frequency for typical buck converters. In addition, commercial ferrite beads can have self-resonance frequencies as low as 2.4 MHz, e.g. Kemet 1207 and 1007 case sizes. [15] This will overlap with the second harmonic of the typical switching regulator ripple.

2.3.4 **Low-pass LC networks**

Low-pass filters constructed from combined stages of inductors and capacitors are popular as power supply ripple filters. This allows a single added LC-product area to give an extra 40dB/decade attenuation when added as a second stage to Figure 2-3 as opposed to just 12dB from the octave reduction in the corner frequency gained by making the existing storage LC stage twice as large in the example of doubling the LC values. Large attenuations at the ripple fundamental can be achieved by having a sufficiently high-order filter and placing the cut off at a low enough frequency. The penalty for this arrangement is that the LC product increases in an inverse square law fashion relative to the decrease in the cut off frequency. A second order filter can give an extra 40dB of attenuation by moving the cut off frequency down one decade. But this requires the LC-product to be one hundred times larger LC product. Inductance and capacitance values are linearly related to volume. This type of filter is not lossless in practice. Voltage is dropped across the series resistance of the inductor. A larger inductor will offer a proportionately larger series resistance and incurred voltage drop.

The use of more optimised passive filters, including coupled-inductor techniques to reduce inductor volume is covered in section 5.1

2.3.5 **Feed forward ripple cancellation schemes**

Many forms of feedforward ripple-cancellation have been presented in the literature [16], [17], [18]. There have been novel schemes presented that are applicable to linear regulation, switching regulation and rectification. They all use variations of the basic scheme presented in Figure 2-12.

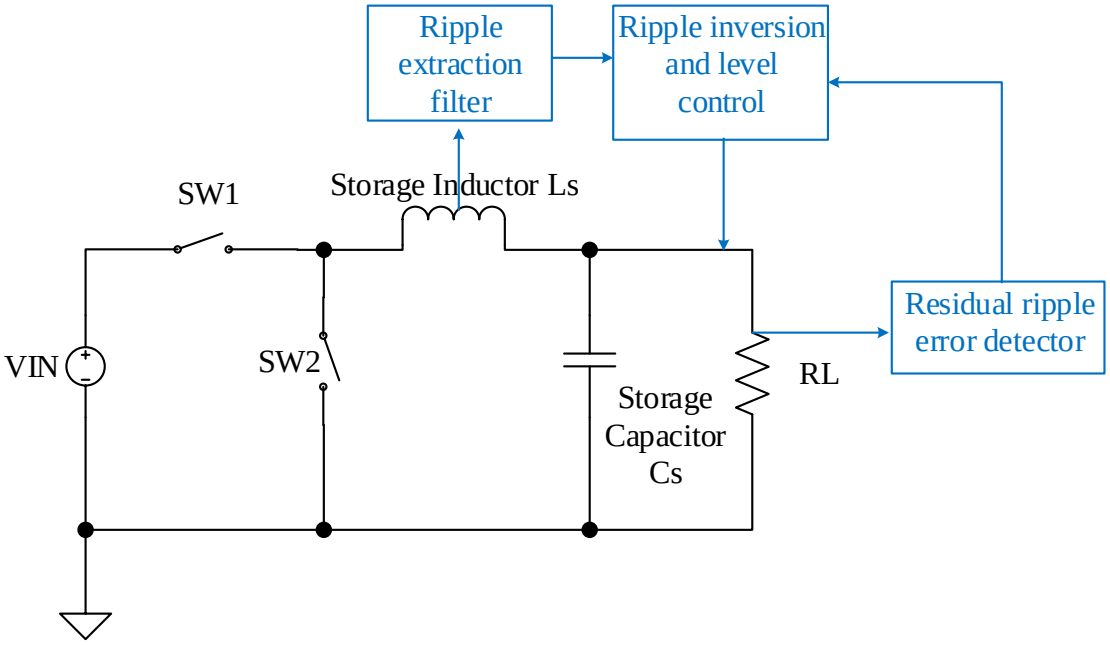


Figure 2-12 Generic feedforward ripple-cancellation technique

In [16] , [18] the ripple extraction and inversion steps are done by replacing the storage inductor, Ls, by a transformer and the level control step is done by adjusting the values

of an added additional inductor and capacitor. In [17], the ripple extraction filter, level control and error amplification are all done by amplifier circuits.

Experimental results presented by [18] for a buck regulator show a 30 dB ripple reduction at a cost of two additional inductors and one additional capacitor. In the case of a linear regulator results are presented by [17] to show a 27 dB reduction in ripple at 1 MHz at a cost of three additional amplifier circuits

2.3.6 **Comparison of the techniques available to reduce power supply ripple**

Technique	**Achievable ripple atte**	**Penalty**	
	for a 1 MHz fundamental		
High performance	-60 dB	1 volt dropped	Note 1
linear regulator		as heat	
20 phases of	-26 dB	Complexity of	Note 2
multi-phase buck		20 phases	
Passive low pass	-40 dB	Large LC product	
(second order example)		physical size to place pole at 100 kHz	
Ripple cancellation	-30 dB	The inductor	Note 3
using coupled inductor		area/size triples	
techniques			
Ripple cancellation	-27 dB	Three additional	Note 4
using active circuits		amplifier circuits	

Table 1 Comparison of different post-regulator techniques to attenuate power-supply ripple.

To construct the table shown in Table 1 comparing the popular ripple-filtering methods used currently the following assumptions and calculations were made.

1. The linear regulator was, as of June 2016, , the best available linear regulator specified for AC PSRR. [13], [19].
2. In calculating the ripple cancellation benefits of 20 phases of multi-phase regulation it was assumed the duty cycle would vary between 40% and 60% through PWM action in response to load transients [12].
3. The passive low pass was taken as a second order LC with the theoretical -40dB / decade attenuation after the corner frequency.
4. The results achievable with both active and passive ripple inversion and cancellation techniques were from [16], [17], [18].

2.4 Chapter Summary

This chapter discussed the ripple content present on a switching regulator output. The dependence on the voltage divide ratio of the relative energy in the fundamental to the even order harmonics was considered. An instance where this spectral content adversely affects an high performance ADC was illustrated. The common techniques used to filter this ripple were outlined.

Chapter 3 Power-supply noise sensitivity of various mixed-signal loads.

The main aim of this chapter is to explore the sensitivity of mixed-signal loads to power-supply noise in the context of the information on power supply output spectral content presented in Chapter 2. These two chapters will then go towards defining the problem to be solved. Subsequent chapters will present various novel techniques to solve the problems outlined in this chapter.

3.1 Introduction.

The sensitivity of analog to digital converters, "ADCs," and digital to analog converters, "DACs, to AC content on the power supply is not widely known and understood. To reduce the number of variables, it is normal that simulations run during the design of a data converter assume the supply is a steady DC source with no AC content. In contrast, frequency generating devices such as PLLs are known to be highly sensitive to power-supply noise and have been the subject of more study [20].

In this section, representative examples of modern ADCs, DACs, RF PLLs and Operational amplifiers are tested to establish their sensitivity to power supply borne ripple. The context is that as shown in Chapter 2, a switched-mode DC/DC power supply regulator will produce a dominant ripple component with the major portion of its energy at the fundamental frequency. That frequency will typically lie between 500 kHz and 2 MHz for modern switching regulators. Broadband noise is not considered

in this study because it has been shown in Chapter 2 that it is of far lower energy than ripple on a typical switching regulator output.

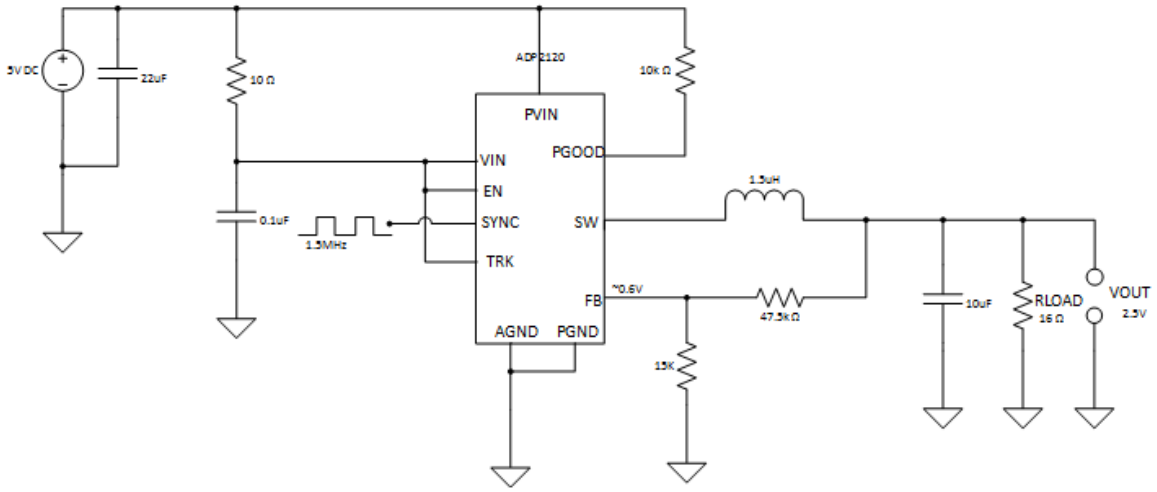


Figure 3-1 Typical buck switching regulator used in a 2:1 divide ratio [21]

For a 1 volt reference, an overlay of the LSB size of representative ADC architectures on a typical switching regulator output spectrum

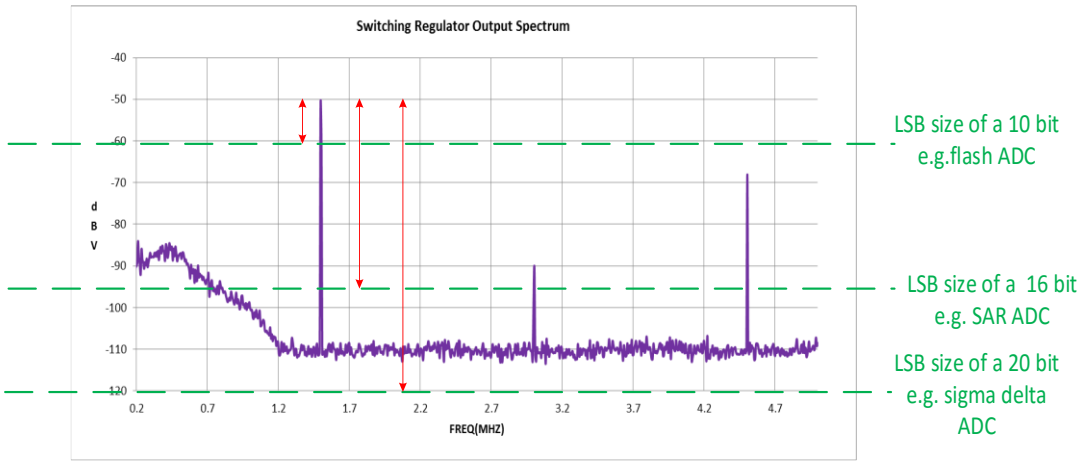


Figure 3-2 An overlay of the typical LSB size by ADC architecture on a typical switching regulator spectral output with a 1.5 MHz switching frequency

Figure 3-2 shows the output spectrum of a typical switching regulator shown in Figure 3-1 with the state of the art LSB size of different data converter architectures, given a 1 V reference, “Vref”, overlaid. (It is accepted in this plot that the output voltage range can be larger than Vref but that is balanced against the maximum permitted noise being set at a full LSB, which is optimistic. It can be seen from this plot that commonly used 20 bit sigma-delta converters require in the order of 70dB rejection or reduction of the fundamental ripple whereas flash may require as little as 10dB. This fact focussed the work presented in this chapter towards sigma-delta ADCs as they represent the greatest challenge for power supply pre-conditioning.

3.2 AC PSRR

The measurement used to characterize a data converter's sensitivity to power-supply noise is AC Power Supply Rejection Ratio (AC PSRR). It is defined here as 20 log (Vout/Vin) where Vin is the measured supply voltage variation and Vout is that resultant measured artefact in the device output. To measure AC PSRR of an ADC or DAC a single frequency tone is coupled onto the power supply and the data converter output is examined for the amplitude of that test tone that has leaked through from the power supply to the signal path. In the case of an ADC an FFT is run on the data stream. In the case of a DAC an analog spectrum analyser is used to measure the output.

As the test tone frequency is increased its level needs to be either maintained constant or measured and noted for each frequency step taken. Reflections from mismatched loads, resonances of passive components and the increased attenuation offered by the decoupling components on the converter under test all contribute to cause a change in test tone amplitude at the converter power supply input as the test frequency is swept.

3.3 ADC sensitivity to power-supply noise

ADCs are used throughout the entire spectrum of electronics applications today, from the very low frequency, very high accuracy/resolution needs in weigh scales used to weigh single bank notes through to digitizing SHF carriers in radar. The three primary ADC architectures in use are sigma-delta for low speed / high accuracy, SAR, for

medium speed / medium accuracy and flash for the highest speeds but with less accuracy.

ADCs operations generally comprise a signal acquisition phase where the signal to be converted is sampled followed by a comparison phase where that acquired signal is compared to a fixed voltage, or ground in the case of a sigma-delta integrator. Layout designers attempt to use mirror image layouts so that the level of Vdd coupling will be equal onto both inputs of the comparator. However, even a typical fF mismatch is sufficient with MΩ input impedances to create a pole in the frequency region where switch-mode power supply ripple lies. A 1 fF difference in gate capacitance of a 50 MΩ input will cause a 3 MHz pole. Device differences involved are below the resolution of present day parasitic extraction capabilities [22].

Each architecture has its own different response to power supply interferers. SAR and flash are similar but sigma-delta is quite different because there is more frequency domain signal processing and consequent opportunities to both completely discard troublesome interferers but also to accidentally alias them back into a high resolution zone where they are above the noise floor and ruinous to the conversion accuracy.

Three representative modern CMOS ADCs were chosen to characterise AC PSRR for this study. The objective was to understand and quantify the interference that typical power supply ripple on the ADC power supply input would add to the ADC output.

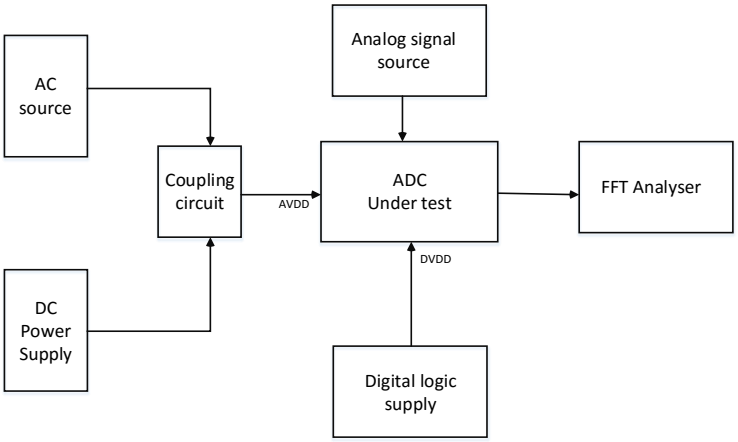


Figure 3-3 Conceptual block diagram of system used to characterize ADC AC PSRR

A representative block diagram of the setup used to characterize an ADC for AC PSRR is shown in Figure 3-3. A test tone is injected onto the power supply through an AC coupler which is used to minimize reflections. Its magnitude is maintained constant at the ADC as the frequency is swept over the frequency range of interest. It is necessary to override the increasing attenuation offered by the supply-decoupling capacitor, as the decoupling component is not the device under test, rather the ADC itself. The interference from the single applied frequency may exhibit dependence on the magnitude and frequency of the signal being converted so the signal to be converted will need to be a constant. This statement applies to all the AC PSRR tests across different device types, such as amplifiers, synthesisers, digital to analog converters, etc. presented in this chapter

3.3.1 **SAR ADCs.**

A SAR ADC comprises a loop that has a successive approximation register, a DAC, a reference and a comparator as shown in Figure 3-4.

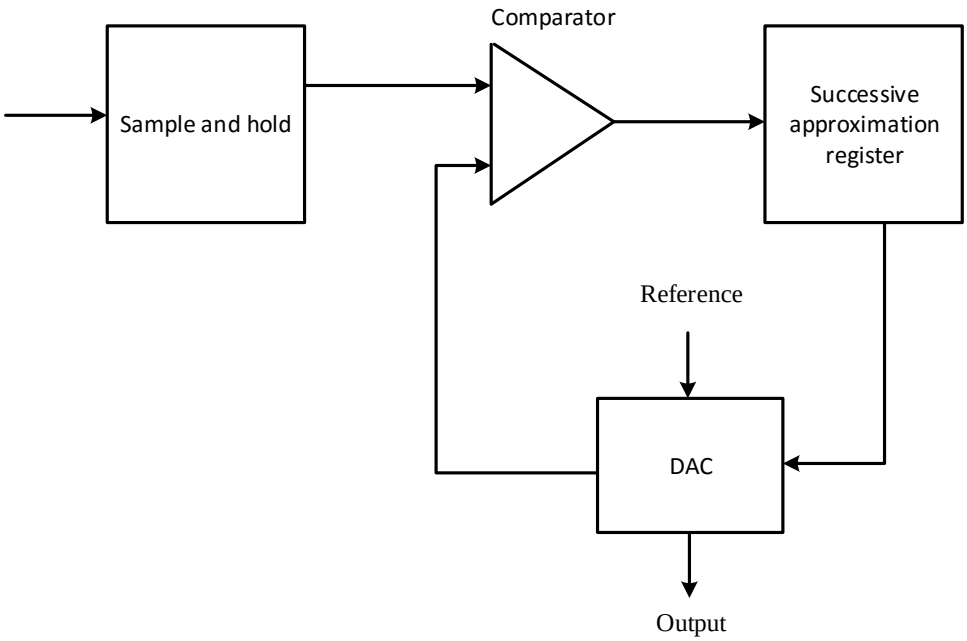


Figure 3-4 SAR ADC concept block diagram

Once the signal is acquired by a sample and hold circuit, each DAC bit is tried for comparative size, consecutively starting with the MSB and working down to the LSB. The SAR ADC looked at in this study is a very common architecture that uses two opposite polarity capacitor DACs followed by a preamplifier and a regenerative latch comparator [23].

During the signal acquisition phase shown in Figure 3-5 half the DAC capacitors are connected between ground and the analog input while the remaining half are connected between the supply and the analog input. Power-supply noise stored on the DAC capacitors during this differential signal acquisition phase will subsequently be cancelled during the conversion stage because half the Vdd-connected capacitors are

switched to Vref + and half to Vref -. thereby cancelling out the interferer potential that existed between Vdd and ground.

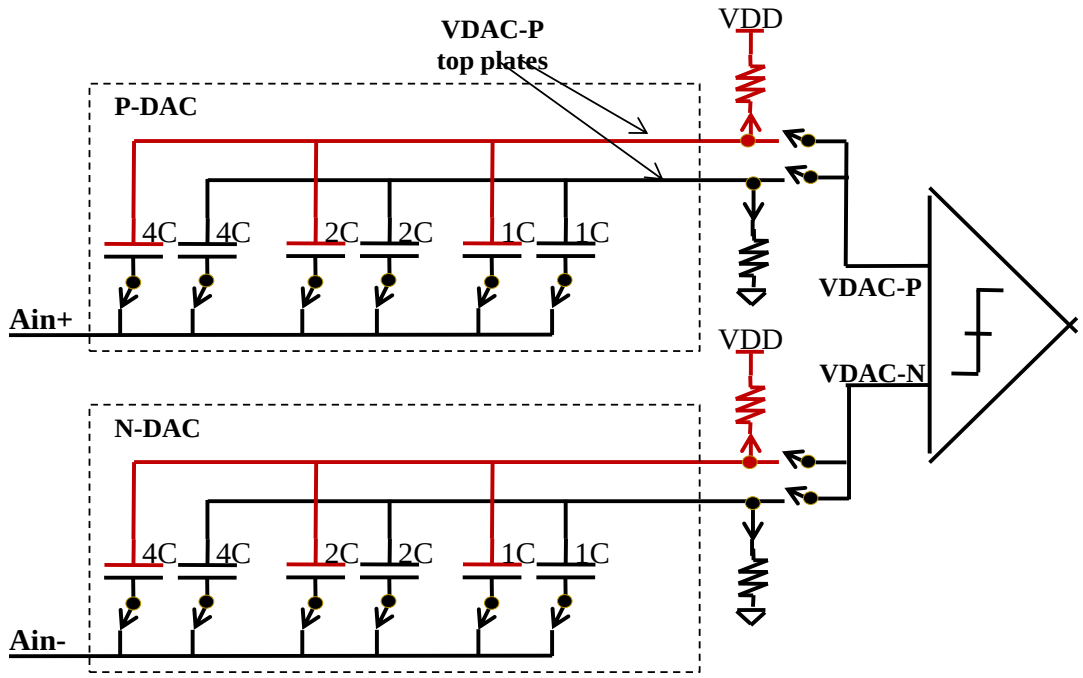


Figure 3-5 SAR ADC in differential signal acquisition phase

However during the bit trial phase shown in Figure 3-6 the two different sets of DAC capacitors are connected between the reference and the comparator inputs. At this time noise on the supply will couple though parasitic paths onto the preamplifier for the comparator causing an ADC error.

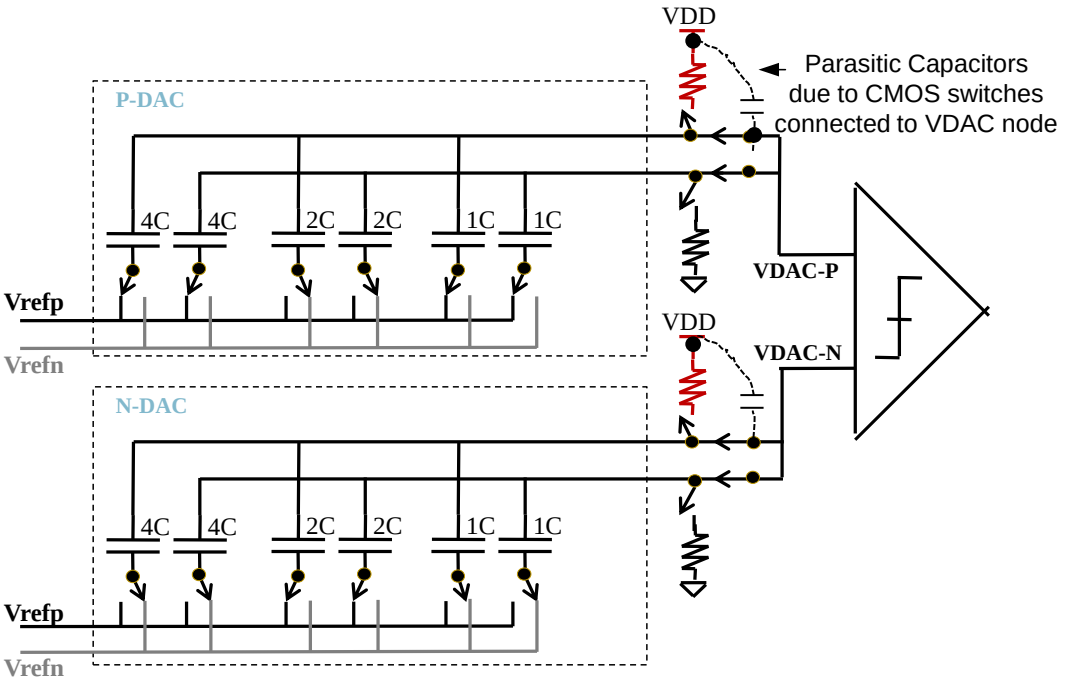


Figure 3-6 SAR ADC in bit trials phase

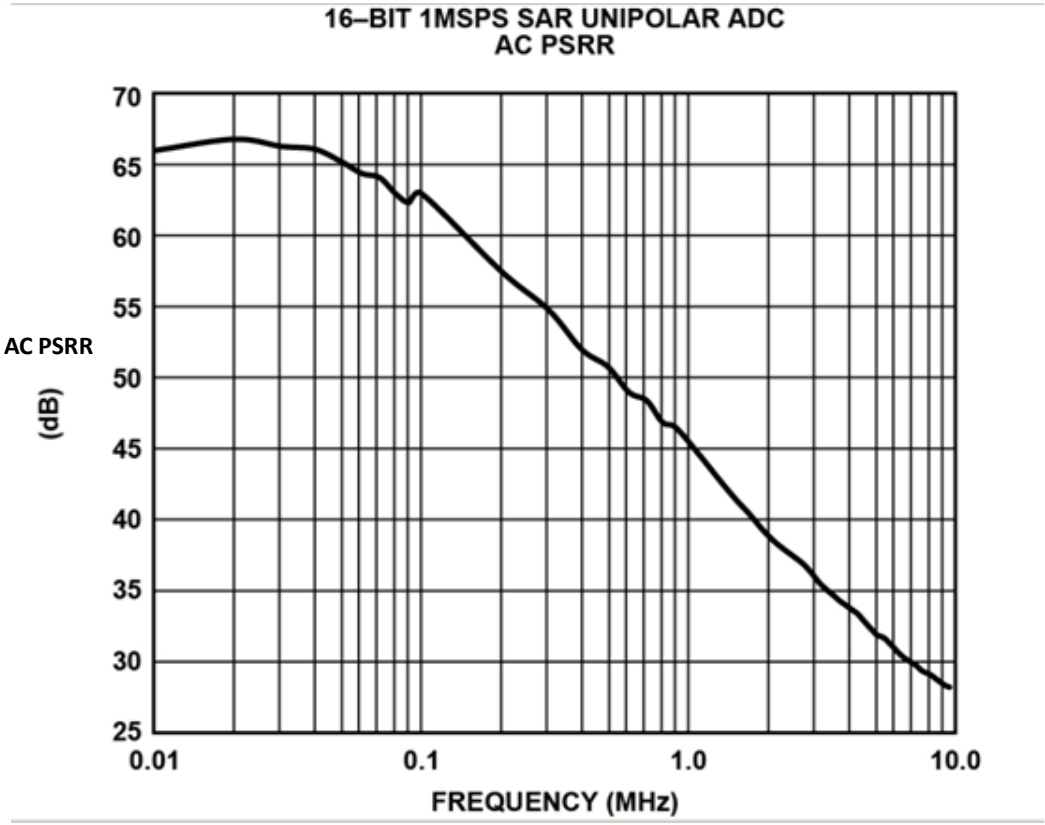


Figure 3-7 AC PSRR of a 16 bit SAR ADC with 1MHz Fconvert

Figure 3-7 shows the AC PSRR plot of a modern 16 bit SAR ADC with a 1 MHz conversion frequency. Note that the rejection seen by the interfering noise will be aliased down to DC at integer multiples of the sampling frequency (i.e.1,2,3,4…MHz ripple frequency). However this is not drawn in this plot for clarity. The plot is constructed by joining points measured at non-integer multiples of Fsample (i.e. Focnvert).

A single pole at 80 kHz is seen. Whilst this ADC has a native rejection of 67 dB for power supply frequencies up to 80 kHz. it will only reject frequencies in the region from 1 to 2 MHz, (where the switching regulator ripple fundamentals typically occur), by 45 dB or less. The native rejection of this modern SAR ADC looked at, does not map well against the switching frequencies typically used in modern switching regulators. Their maximum rejection range is below the fundamental clock frequency of the power supply.

3.3.2 **Flash ADCs**

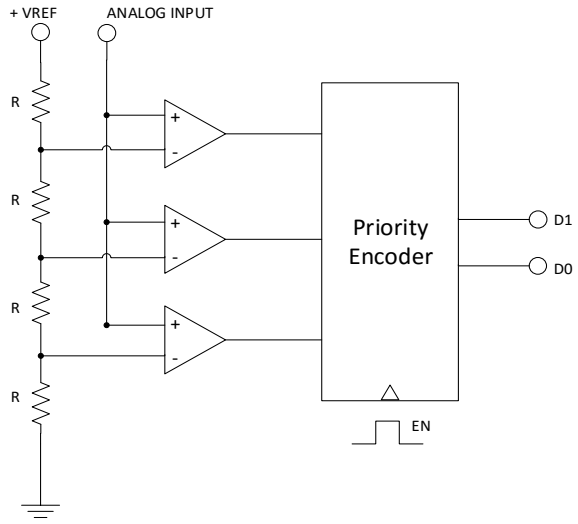


Figure 3-8 Simplified 2 bit flash ADC

Flash or Direct Conversion ADCs use a parallel string of comparators to simultaneously compare the analog input to all 2^{N-1} possible voltage divides of the reference. Figure 3-8 shows a conceptual diagram of a two bit flash ADC. Pipeline ADCs are a derivative of Flash where a number of consecutive stages reuse the one block of comparators, reducing the number of comparators required. Like all ADCs there is a signal acquisition phase and a conversion phase. Similar to SAR ADCs, power-supply noise coupling to the acquired signal acquisition or comparator circuits will result in an ADC output error.

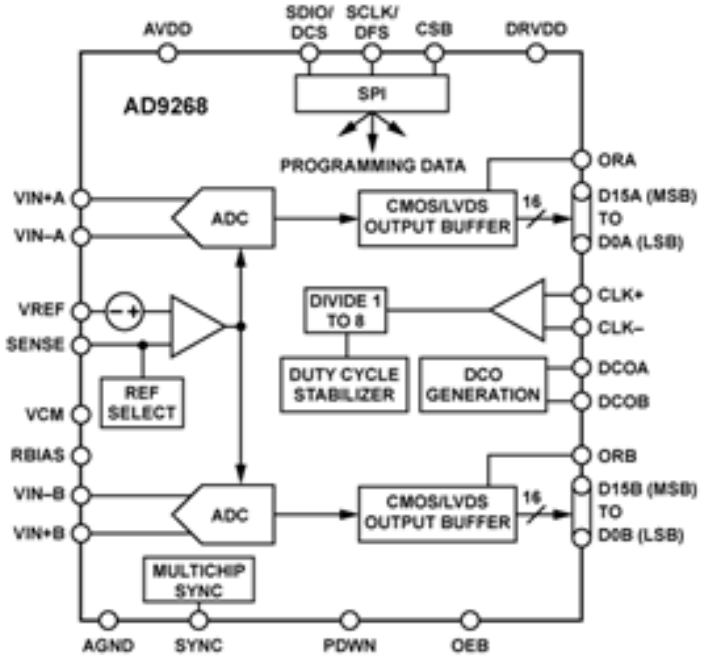


Figure 3-9 Dual, pipelined 16 bit 125 MSPS ADC [24]

Figure 3-9 shows a modern dual, multi-stag pipelined ADC designed for application in the IF region of cellular base station receivers used for this test.

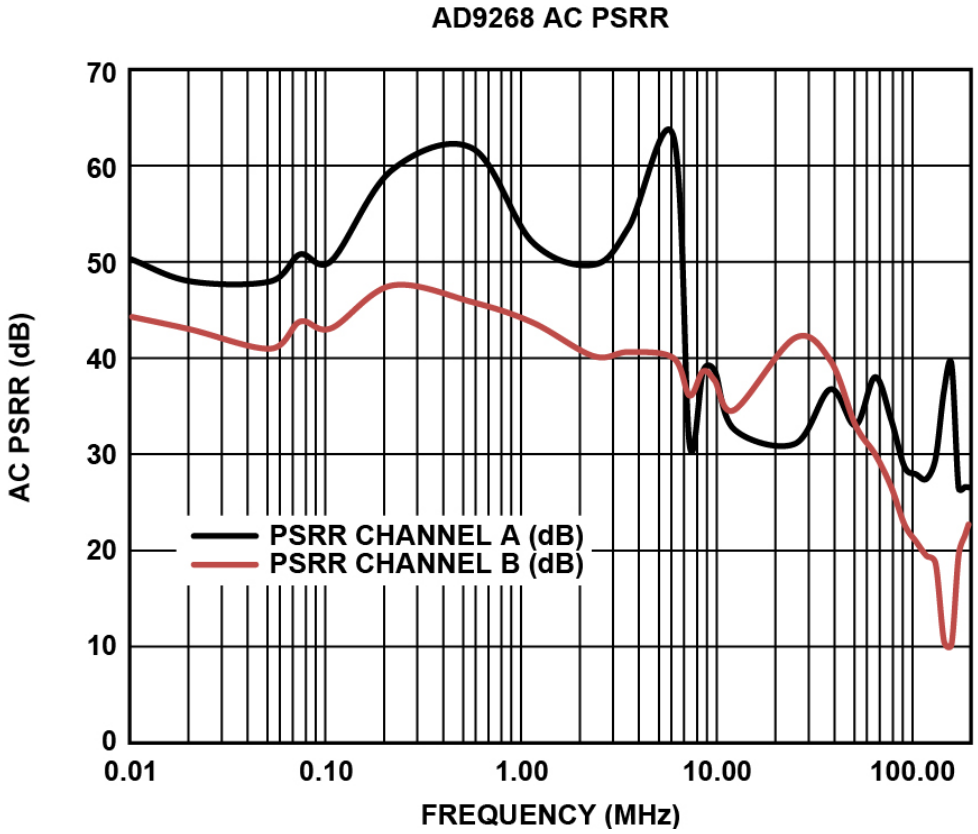


Figure 3-10 AC PSRR for a 125 MSPS pipelined flash ADC

Figure 3-10 shows the measured AC PSRR of a dual, pipelined 16 bit, 125MSPS ADC. Although it is a different architecture and process to the 16 bit SAR ADC shown in Figure 3-7, it has a similar pole location. The first pole in the response occurs in the region of 1MHz and falls from approximately 50dB at 20dB/decade. Both the specific SAR and Flash architectures looked at here exhibit similar levels of rejection to 1MHz test interferers on their power supplies.

3.3.3 **Sigma-Delta ADCs.**

A sigma-delta ADC uses an integrator to drive a comparator creating a voltage to pulse frequency converter.

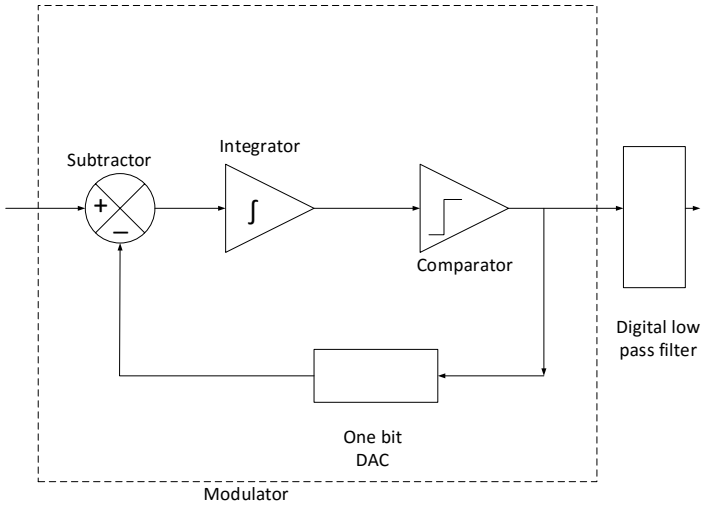


Figure 3-11 Conceptual sigma-delta ADC

A conceptual diagram of a first order sigma-delta ADC is shown in Figure 3-11. Oversampling is used which allows a digital filter following the modulator to discard much of the spectrum above the bandwidth of interest. The integrator causes the quantization noise to be shaped [25] such that it is pushed to higher frequencies where the low-pass filter rejects it. The result is a high resolution capture of a narrow band. However, the accuracy of the result is limited by the errors introduced in or before the modulator that either originate within the retained frequency band or elsewhere at a frequency that is aliased back down into the frequency band of interest.

A first-approximation plot can be constructed showing the attenuation seen by an interferer on the power supply of a discrete time sigma-delta ADC relative to the frequency of the modulator, the shaped quantization noise and the digital filter response. Figure 3-12 shows the regions of susceptibility to power supply borne noise for a discrete time sigma-delta ADC. This theoretical plot is presented now to contextualize actual measured results that follow later in this chapter. It is specific to a double-sampled integrator scheme. A single-sampled integrator would have a flat modulator response in this diagram.

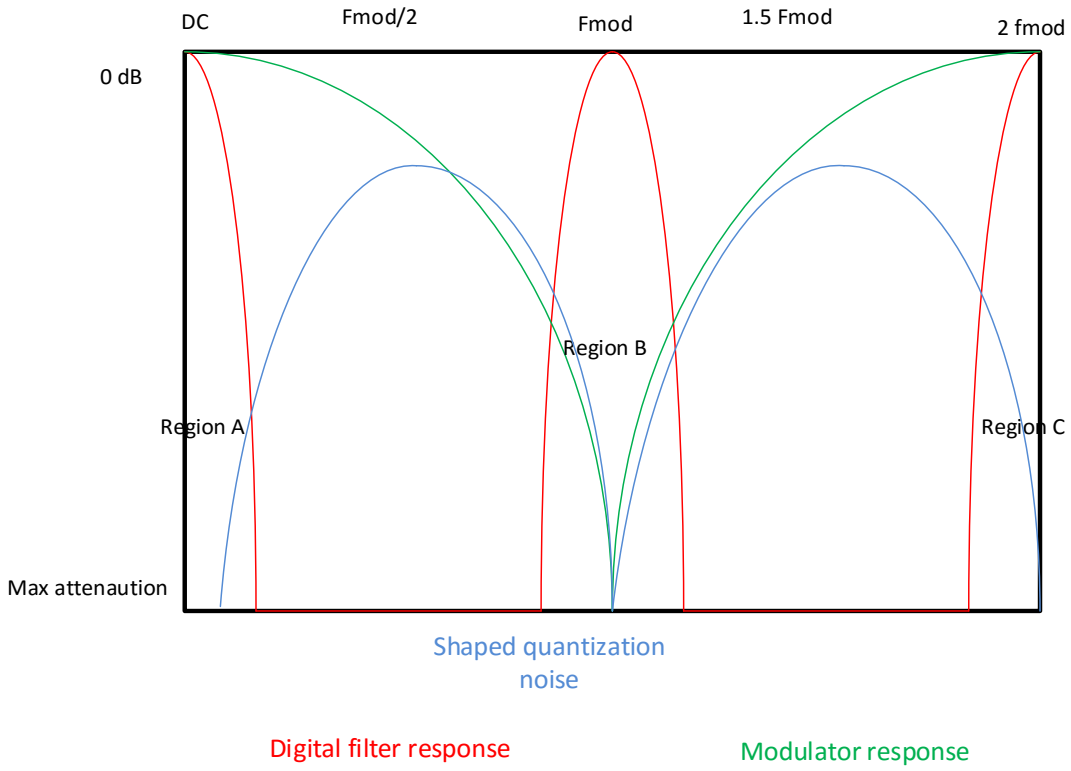


Figure 3-12 Regions of susceptibility of a sigma-delta ADC

Referring to Figure 3-12 the regions outlined are described here.

Region A (DC)

The intended passband of the ADC. Neither the digital filter not the modulator are giving any attenuation. Power-supply noise would get to the output. However, parasitic coupling is at its least effective here and the differential input structures are effective.

Region B (Fmod)

The integrator is running at twice the modulator frequency ,"2 Fmod" and has maximum rejection at the modulator frequency "Fmod". Note that this double

sampling does not mean the quantizer is running at 2 Fmod. It is just sampled at 2 Fmod. However, the digital filter is running at Fmod and so has no rejection, but the high level of rejection of the modulator should suffice.

Region C (2Fmod)

The integrator is sampling at 2 Fmod and will see aliasing. The digital filter is not giving rejection at twice its clock rate. Differential input structures will not be as effective as at lower frequencies as parasitic coupling degrades their effectiveness as the frequency increases.

Figure 3-13 is a measured plot of a 24-bit discrete-time sigma-delta ADC plotted to show the effective resolution in the presence of both power supply and reference noise at varying frequencies. Noise on the reference is measured as a separate case to the supply alone for sigma-delta architectures because the interaction with supply noise coupling onto the sigma-delta reference are more complex than for a SAR or Flash as the effect of shaped quantization noise is an additional complexity The red trace in Figure 3-13 refers to the power supply interferer on AVdd only. The green trace refers to the interferer on the reference and analog inputs only. It was useful to separate them out to understand what would happen when the ADC is used in a ratiometric configuration with the reference divided down from the analog supply.

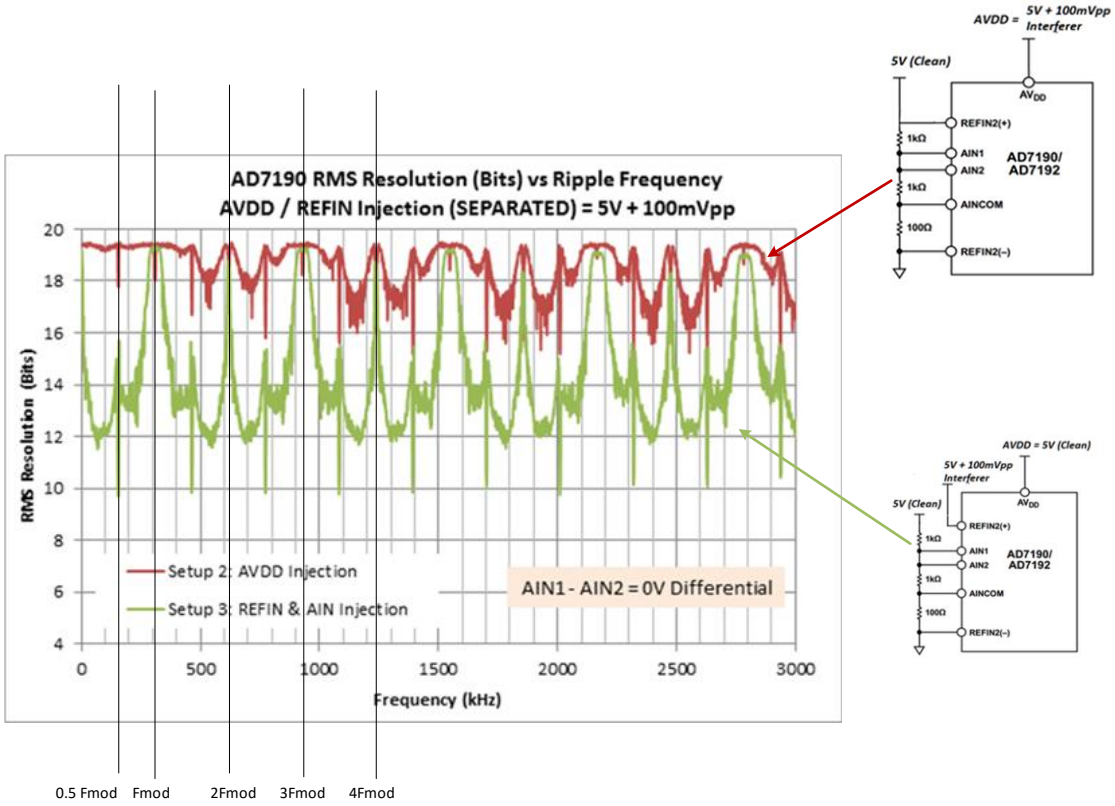


Figure 3-13 Sigma-delta ADC effective resolution versus interference frequency

Effective resolution also known as effective number of bits (ENOB) is calculated from the ratio of the RMS noise to the full scale range of the ADC. A 100 mV p-p interferer was coupled onto both the power supply and the reference at the ADC pins at separate times. For the given test conditions with an ideal power supply, 19.5 bits was the specified effective resolution of the ADC under test. A zero volts signal was applied to Ain, the signal to be digitized. The modulator frequency was nominally 307.2 kHz.

When the power supply interference is on just the supply pin (red trace) a correlation is seen to regions of theoretical susceptibility shown in Figure 3-12. Note that at exactly 2 Fmod and further even multiples, the aliases are transposed to DC, but either

side of it performance reduces sharply. At Fmod and odd multiples, there is a wider area of good operation, as predicted.

But when the power supply interference is coupled to the ADC reference pin as would be the case in ratiometric operation of the ADC, (green trace), the ADC is far more sensitive to noise coming from the power supply.

Referring to Figure 3-13 the regions in the measured values are described here.

From DC to 0.5 Fmod

There is a rapid fall off in ADC performance from 19.5 bits to 10 bits. This is caused by mixing of the internal quantization noise of the modulator with the interferer on the reference. A low-pass sigma-delta modulator has a low level of quantization around DC, but this increases at a rate of 20 N dB, where N is the order of the modulator , up to 0.5Fmod. The device under test here has a fourth order modulator, i.e.an 80dB/decade increase in quantization noise. Therefore, higher frequency interferers are mixing with higher quantization noise, which leads to worse overall ADC performance. The measured decrease in effective resolution in the first 100 kHz was 6 bits / decade as shown in Figure 3-14. This was consistent across 20 mV to 100 mV of ripple and different Ain signals to be digitized from 0V to 2. 4V.

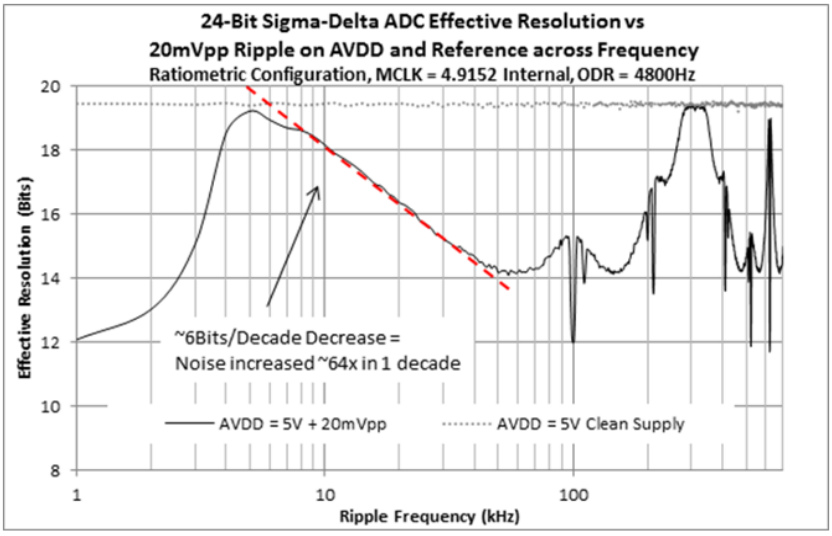


Figure 3-14 Measurement of decrease in effective resolution tracking quantization noise shape

0.5 Fmod.

There is a large negative "spike" in noise performance for frequencies very close to 0.5 Fmod. This is because a 0V input on the sigma-delta modulator results in a large frequency content at 0.5 Fmod. The modulator output will be a single bit sequence of 1,0,1,0,1,0 which gives a strong component at 0.5Fmod.

Quantization noise is also high at 0.5 Fmod so an interferer at this frequency causes the biggest performance impact.

0.5 Fmod to Fmod.

The modulator operates at a frequency of Fmod, so its quantization noise frequency is symmetrical about 0.5 Fmod. This would suggest a mirror image from DC to 0.5 Fmod would be observed from 0.5 Fmod to Fmod. The actual response is a little worse below 0.5 Fmod. This is because the modulator samples on both clock edges and

operates on an average of the two samples. That provides increasing attenuation of the interferer as the interferer frequency is increased, causing less impact on the ADC performance.

Fmod.

The best performance of the ADC is seen in a region around Fmod. That is related to the fact that the sampling frequency equals 2 Fmod. The ADC and reference are both sampled at a rate of 2 Fmod. A running average-by-2 of the current and previous samples is effectively performed, before the input and reference samples are passed on to the later stages of the sigma-delta-modulator, which operate at a rate of Fmod. An average-by-2 operating at a sample rate of 2 Fmod provides strong rejection of any signal around Fmod. The average-by-2 is performed prior to the sigma-delta modulator. Therefore an interferer at Fmod is notched out regardless of how the sigma-delta modulator subsequently processes the signal.

2 Fmod.

The ADC in this device samples its analog and reference inputs at 2 Fmod so any interferers at that frequency will alias to 0Hz. For a zero volt input signal the ADC accuracy will not be effected. However, aliasing noise down to DC for a non-zero signal to be digitized is undesireable. The response seen immediately either side of 2 Fmod is identical to the behaviour around DC.

Above 2Fmod.

The behaviour mirrors what was seen below 2 Fmod in a repeating sequence, with a period of 2Fmod.

Effect of signal level

A separate test was carried out to examine the effect of the signal voltage magnitude on the interference pattern seen when a power-supply noise interferer is introduced to the reference and supply inputs combined. Figure 3-15 is an expanded view of the case of a 0 V analog input seen in Figure 3-13. A dependency of the amount of noise seen from an interferer on the reference is seen, acting on the voltage present on Ain. This is caused by the interferer on Ain not being completely in phase with the interferer on the reference. At 2 Fmod the ADC is no longer immune to noise on the reference when the input signal level is non-zero.

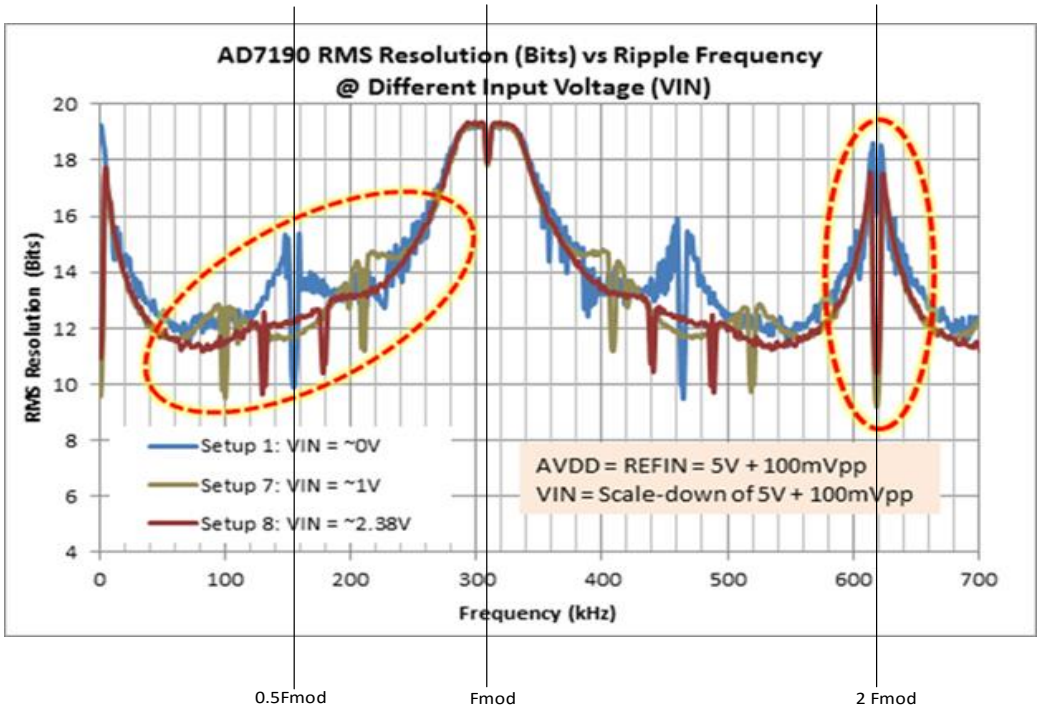


Figure 3-15 Measured effect of the magnitude of the analog signal to be digitized on the sensitivity to supply noise of a sigma-delta ADC

Simulations

Figure 3-16 shows an ADICE (Internal Analog Devices Spice based simulation tool) behavioural model of the sigma-delta ADC measured and shown in Figure 3-16. It was simulated with identical conditions of a 100mV power supply interferer appearing on the reference. It corresponds well to the actual measured result.

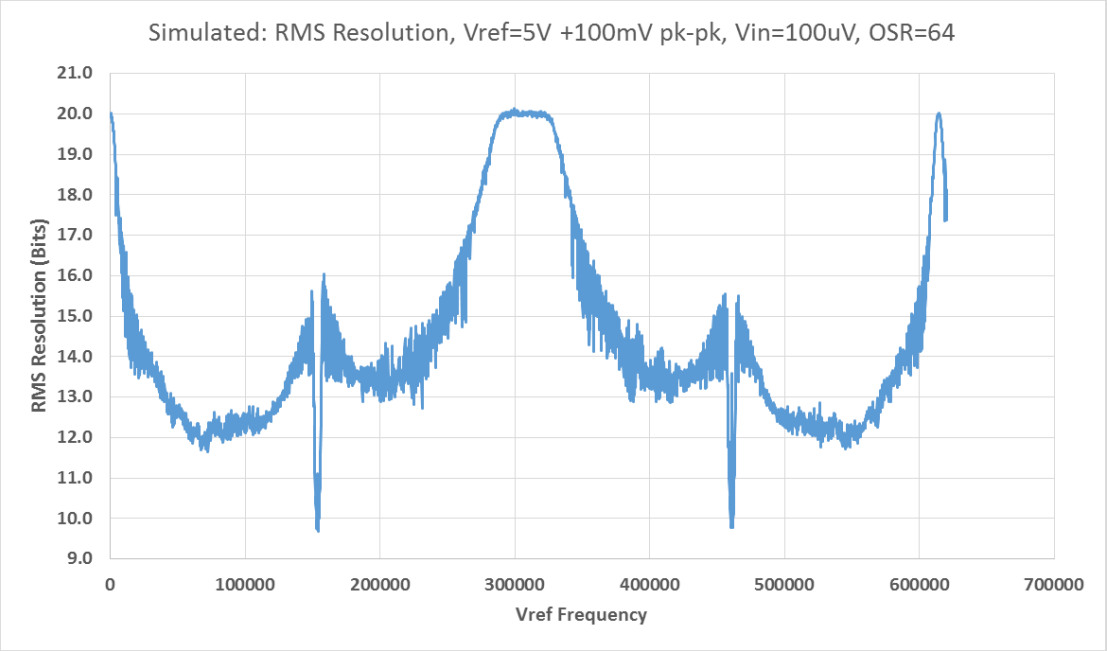


Figure 3-16 Simulation of effect on sigma-delta ADC effective resolution of power-supply noise on the reference.

3.4 DAC sensitivity to power-supply noise

DACs are used across a broad spectrum of applications, ranging from high accuracy DC setting in instrumentation to direct generation of the 20 GHz RF carriers in radio systems. The accuracy required ranges from 8 bits for low resolution, control applications to 20 bits in audio. The most popular DAC architectures used in industry today are resistor network (R-2R and String DAC) for lower speeds and switched current source architectures for RF applications. Sigma-delta DACs are primarily used in audio where very high resolution at a relatively slow speed is required.

While sigma-delta DACs will have some commonality with the aforementioned sigma-delta ADCs, DACs constructed from various topologies of switched resistors, capacitors or current sources differ from ADCs in their likely sensitivity to power supply borne noise. Unlike an ADC, a DAC is “always on”. An ADC momentarily samples the analog world and then generates a digital representation. Noise at the wrong frequency has to be at the wrong time to corrupt the ADC answer. However, a DAC momentarily looks at the digital input and sets a constant analog value to match. Noise of the “wrong” frequency, at any time, on a DAC power supply will get through to the DAC output as an interferer.

Figure 3-17 shows a diagrammatic representation of a two-bit resistor string DAC. Also known as a thermometer DAC, the primary path for power-supply noise to couple will be through the powered elements of the circuit, namely the reference (if it is on-chip), the reference buffer, the DAC switches and the output buffer. This will hold across all DAC architectures and will include other powered elements such as the current source, integrators, etc.

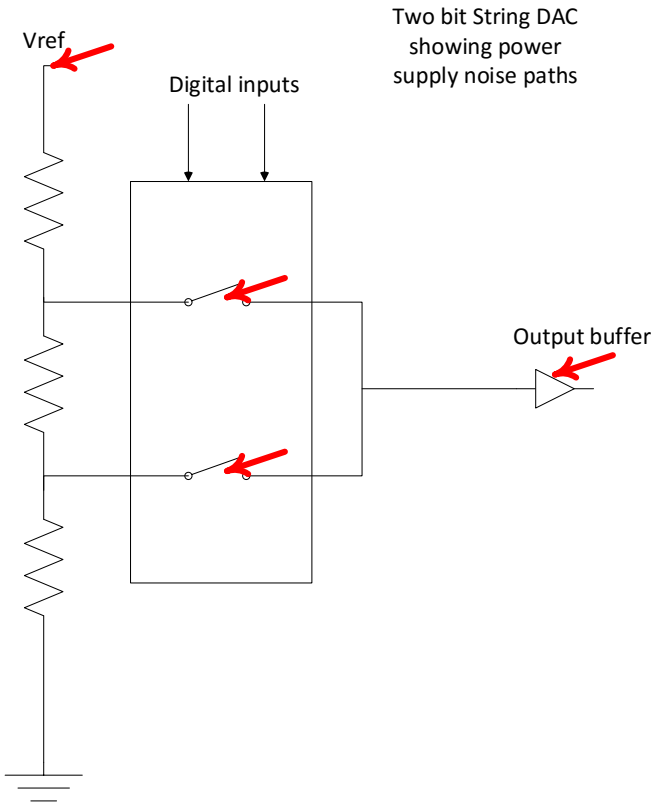


Figure 3-17 Conceptual 2-bit thermometer DAC with red arrows showing elements of high sensitivity to supply borne noise

Three representative modern CMOS DACs were chosen to characterise AC PSRR. The objective was to understand the extent of the interference that typical power supply ripple as seen in Chapter 2 would cause to the different DAC outputs.

Case 1. 20 MSPS 16 bit-quad resistor-string DAC with on-board buffer designed for instrumentation.

Case 2. 250 MSPS 16-bit dual switched current source DAC designed for IF generation in radio.

Case 3. 5.6 GSPS 14-bit switched current source DAC designed for RF carrier generation.

Figure 3-18 shows the generic test setup used to characterise the power-supply noise sensitivity of a DAC. The tests were done by coupling a single frequency onto the power supply pin and measuring the artefact of that frequency on the DAC output using an analog spectrum analyser. Different test criteria were carried out for each DAC to replicate the application for which it was designed. The 20 MSPS device is intended for general purpose use and as such it was appropriate to do a full scan of AC PSRR up to its Nyquist rate. The 250 MSPS and the 5.6 GSPS devices are both intended for generation of one application-specific frequency so those specific applications were examined for power-supply noise susceptibility within that zone of operation.

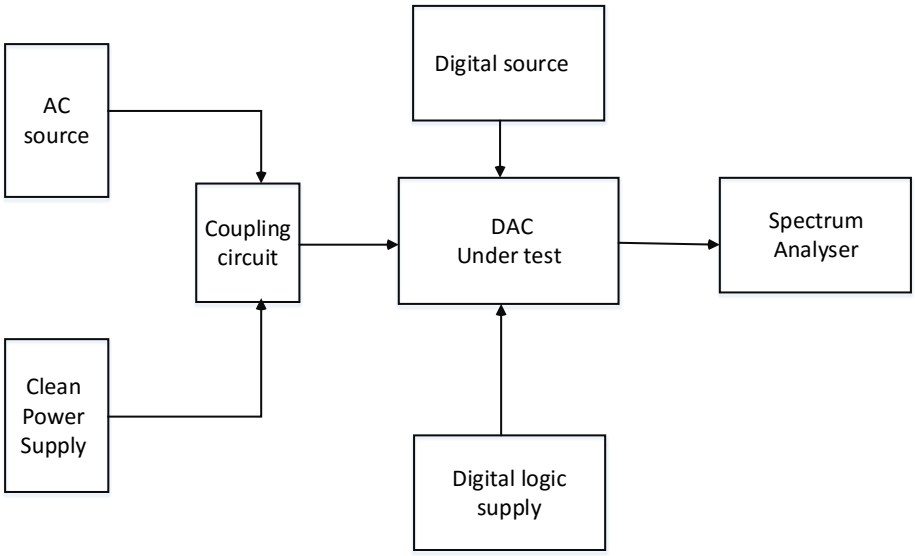


Figure 3-18 Generic DAC power-supply noise test setup

3.4.1 **Power-supply noise tests on a 20 MSPS 16 bit String DAC**

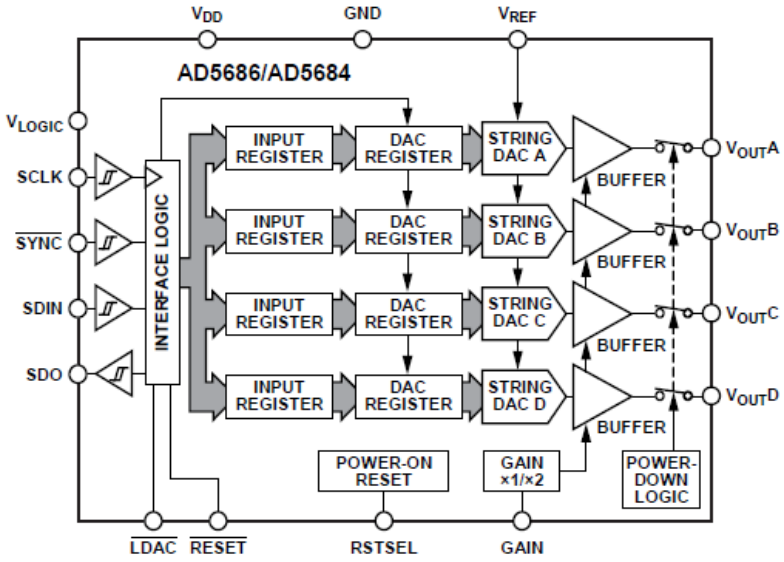


Figure 3-19 20 MSPS 16 bit String DAC [26]

Figure 3-19 shows a block diagram of a modern 20 MSPS 16 bit quad resistor-string DAC with on-board buffer designed for instrumentation applications.

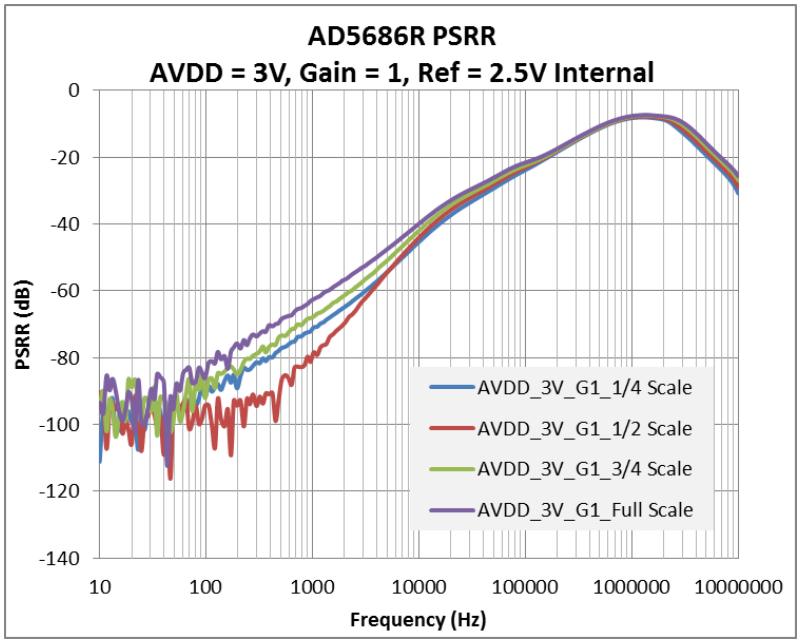


Figure 3-20 DAC AC PSRR measured with AVdd = 3 V.

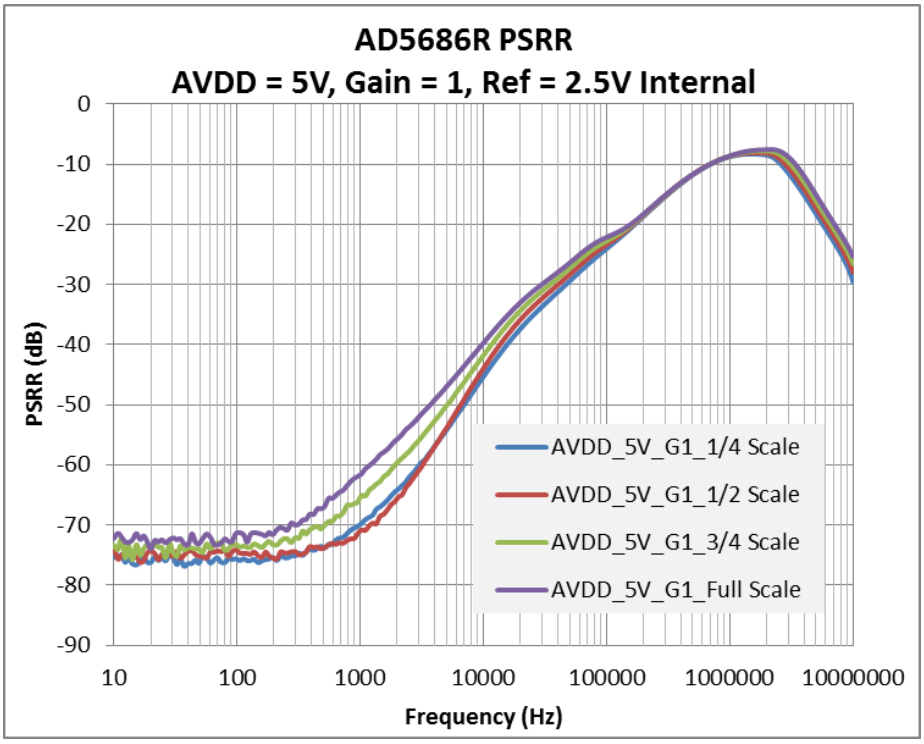


Figure 3-21 DAC AC PSRR measured with AVdd = 5V.

Figure 3-20 and Figure 3-21 shows plots of the power supply rejection of the DAC (including its on board output buffer) plotted for various codes applied to the DAC at both 3 V and 5 V supplies. A pole occurs at approximately 100 Hz at 3 V. In the 5 V plot the pole first appears above the high noise floor at 1 kHz. As the input code is increased, more of the DAC switches are connecting the reference to the output thereby coupling more noise from the reference path with increased code. At 1 kHz there is a 10 dB difference between one quarter scale and full-scale DAC codes, indicating the noise path is related to the internal reference used, at that frequency. However, the difference caused by the code major transitions converges as the test frequency approaches 10 kHz, indicating it is the output amplifier noise path that dominates at this point. With a 3 V supply, the device has gone from 90 dB rejection of a 200 Hz power supply interferer to less than 10 dB at 10 kHz. The shape of this curve is of course reminiscent of an operational amplifier's AC PSRR response but inverted. That is essentially what it is. The DAC designer inserted a low frequency dominant pole to achieve a stable amplifier. This graph suggests that if some additional bypassing can be placed near the output buffer to further attenuate the power supply interferer then this class of DAC would be less susceptible to ripple from a switching regulator.

Figure 3-22 shows a plot taken when the device was operated with a gain of 2 and a 2.5 V reference to deliberately run the on board output buffer out of headroom when a full scale output was called for. There is now no power supply rejection at full scale demonstrating and isolating the role the output buffer plays in rejecting AC on the power supply.

In most cases shown here, half scale shows better immunity to power-supply borne noise than quarter or three-quarter scale. This is because half scale is code

100000...compared to quarter scale at 0001111… or three quarter scale at 1110000…as approximate examples. Half scale has just one switch connected to the reference and thereby couples less power supply noise.

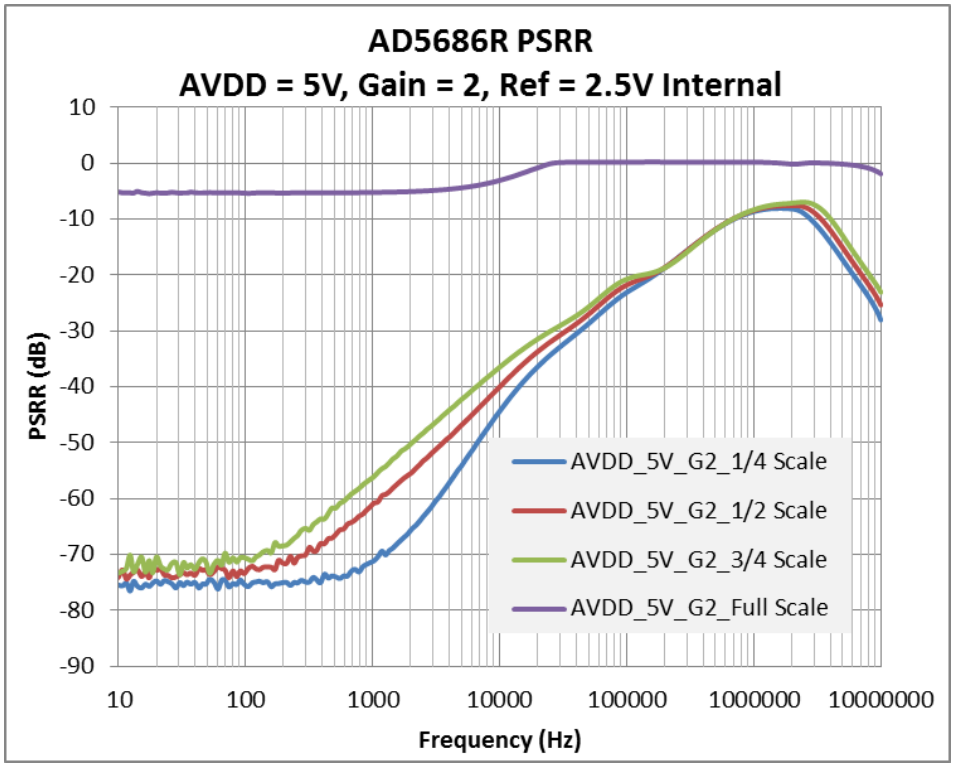


Figure 3-22 DAC AC PSRR measured with AVdd 5V, Gain =2

3.4.2 **250 MSPS 16 bit dual switched current source DAC designed for IF generation in radio.**

Figure 3-23 shows a block diagram of the second DAC device investigated. It is a high speed device, specifically designed for use in cellular radio and uses a switched current source architecture. With a 250 MSPS maximum update rate, its specific application is generation of the 61. 44 MHz Intermediate Frequency used in WCDMA.

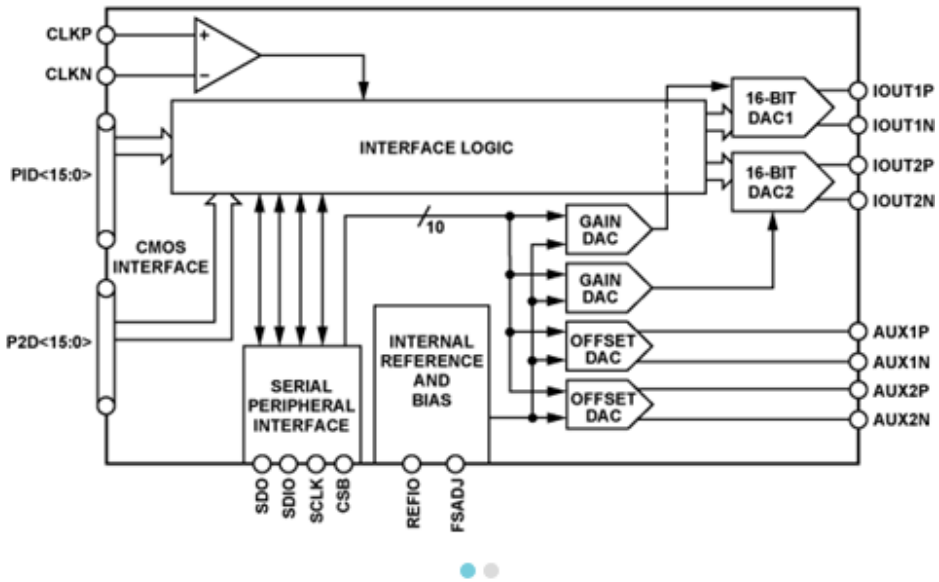
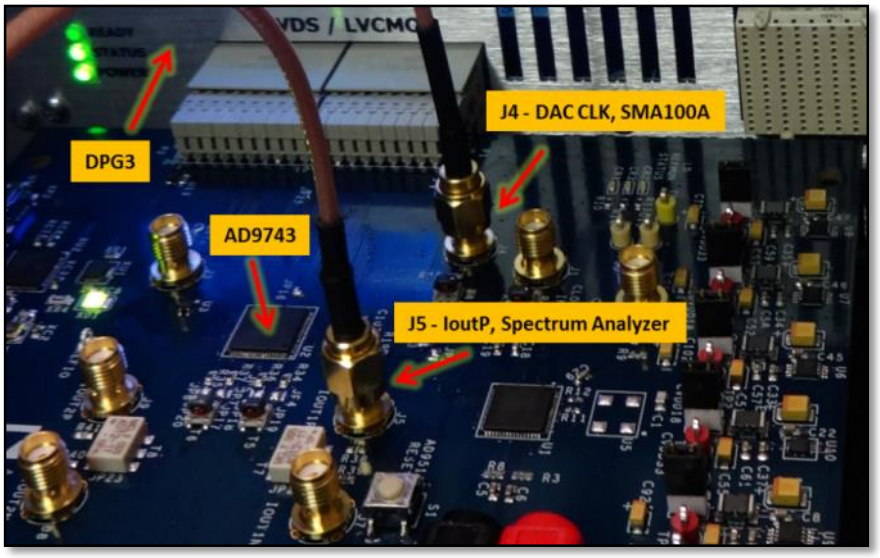


Figure 3-23 Switched current source 250 MSPS DAC [27]

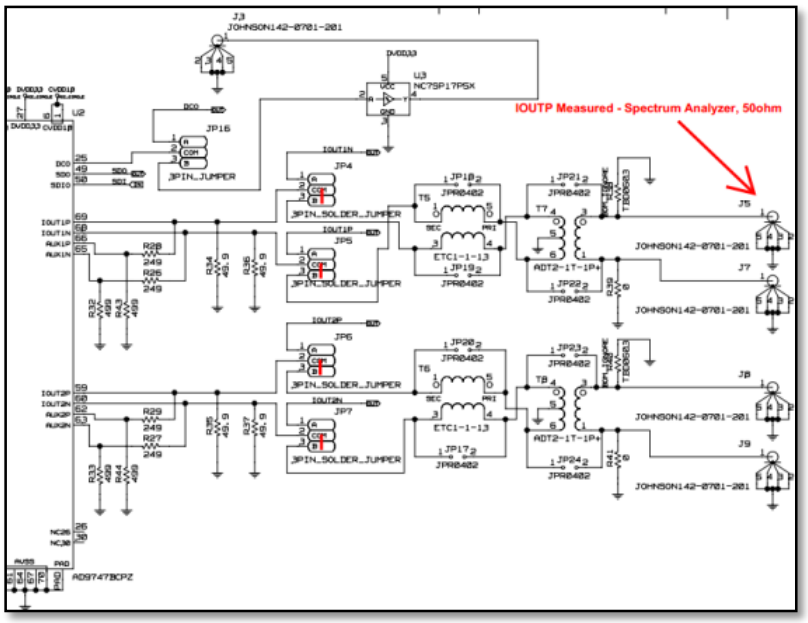
A 1 MHz ripple was coupled onto each of the two power supply rails likely to be sensitive, the analog supply, AVdd and the clock circuitry supply, CVdd, in sequence, at both 100 mV p-p and then 10 mV p-p.

(B)

Figure 3-24 shows the evaluation setup used.



(A)



(B)

Figure 3-24 (A) Evaluation setup for RF DAC power-supply noise tests and (B) schematic.

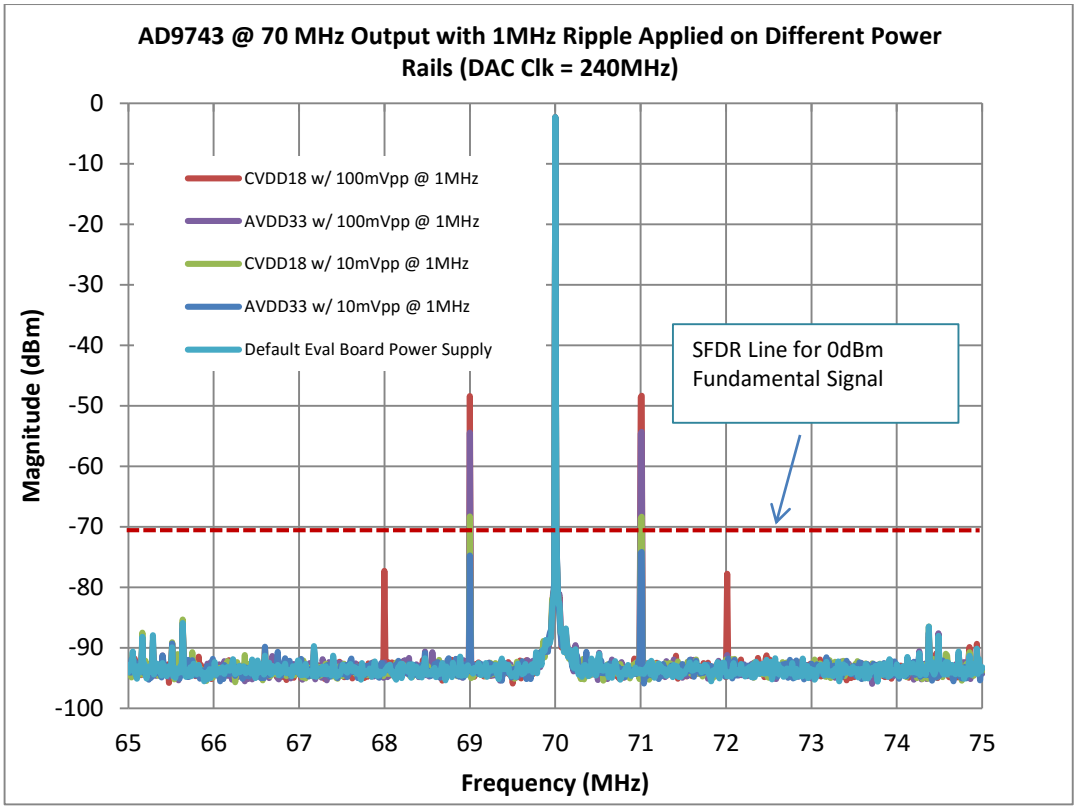


Figure 3-25 250 MSPS DAC output spectrum for various power supply interfers

The manufacturer specifies this device as having a 70 dBc Spurious Free Dynamic Range. This is indicated by a dotted red line in Figure 3-25.

It is seen that power supply ripple at 1 MHz described in Chapter 2 will degrade the device performance, even down to 10 mV p-p interferer amplitude. However, noise on the clock power circuitry did not appear to raise the noise floor as would have been expected.

3.4.3 **5.6 GSPS 14 bit switched current source DAC designed for RF carrier generation.**

The third DAC characterised was a very high speed device that is specifically designed for carrier synthesis in video and cellular transmission systems. Figure 3-26 shows a block diagram of this switched current source architecture device.

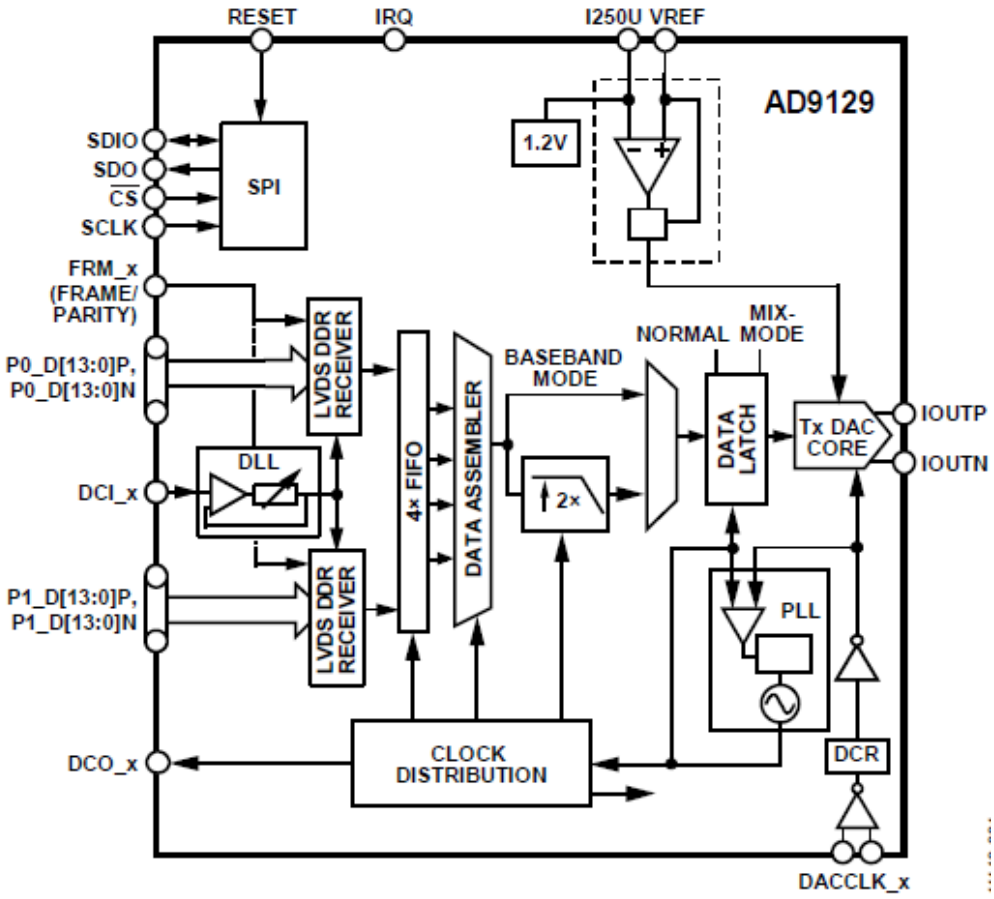


Figure 3-26 Switched current source 5.6 GSPS DAC [28]

The device was tested for power-supply noise artefacts on the DAC output in two different application scenarios with different output requirements.

1. Digital frequency synthesis where the DAC is used to directly generate a single frequency 1 GHz tone.
2. Digital frequency synthesis where the DAC is used to generate a WCDMA 877.5 MHz dual carrier.

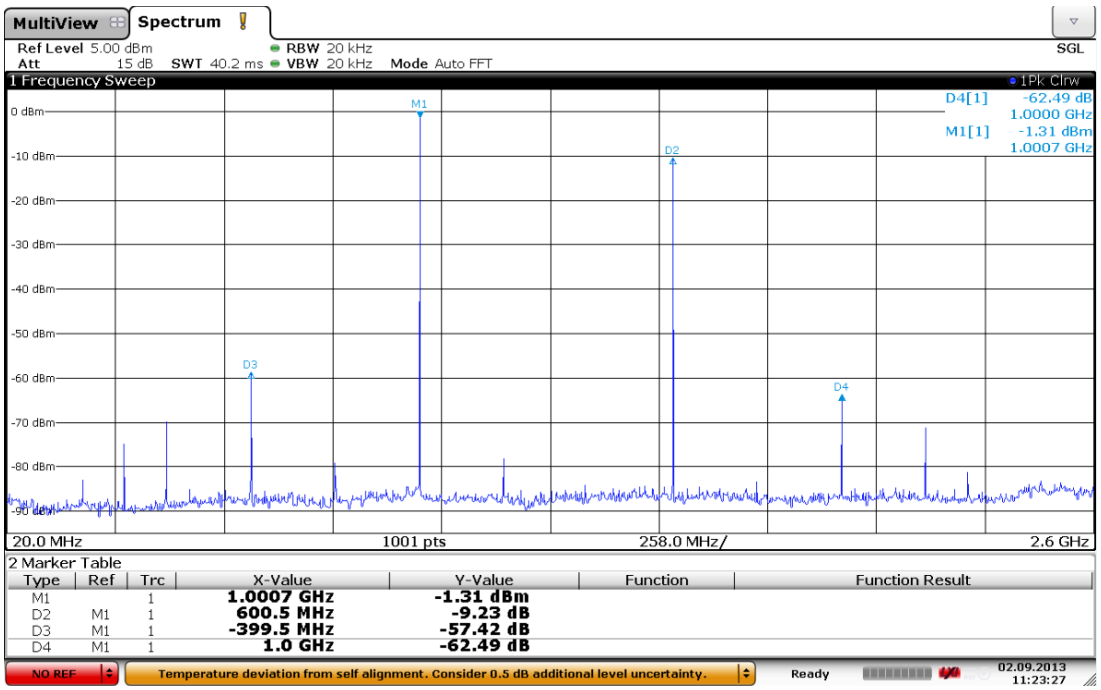


Figure 3-27 Spectral output acquired when 5.6 GSPS DAC is generating a single 1 GHz tone using a linear laboratory supply.

The spectral output when a 1 GHz signal was generated using a linear laboratory supply for Vss is shown in Figure 3-27. Aliased artefacts are noted at 400 MHz and 600 MHz . Subsequently with a 1.4 MHz 100 mV p-p ripple was injected on Vss, with the result as shown in Figure 3-28. In the case of the added power supply interferer, aliases of the 1.4 MHz test tone are seen either side of the 1 GHz wanted tone. The interferers are 40dB below the wanted tone in Figure 3-28 compared to a

noise floor at approximately 87dB in that frequency area with the clean supply in Figure 3-27. Thus there is a loss of 47 dB of dynamic range resulting from a 100mV, 1.4MHz ripple on the power supply.

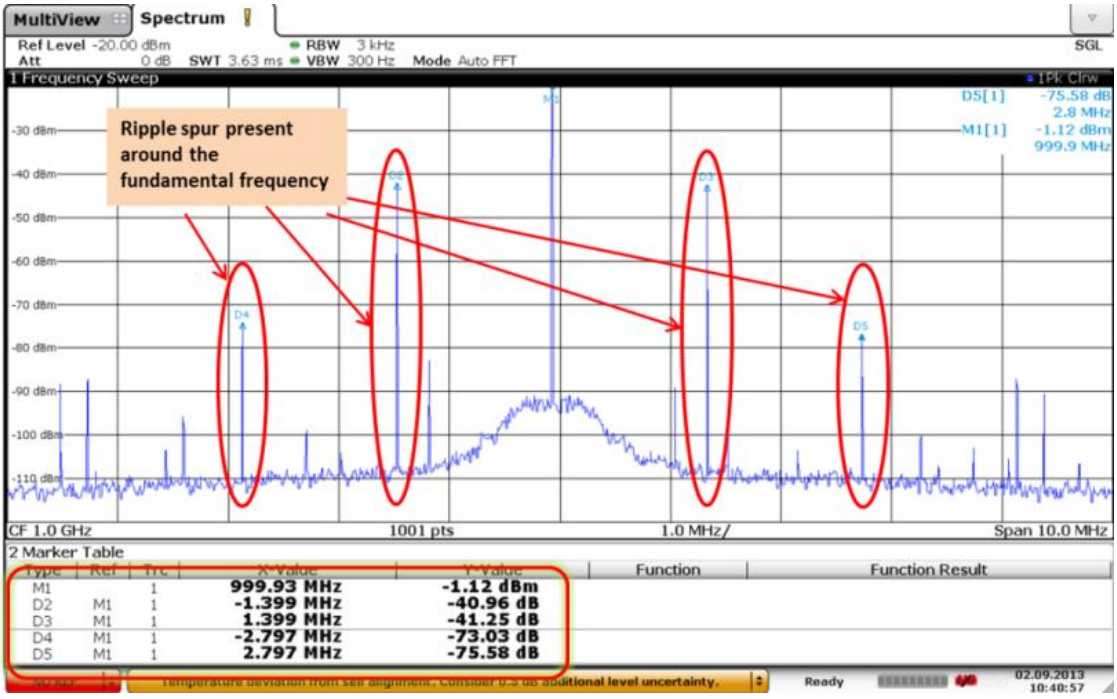


Figure 3-28 Spectral output when 5.6 GSPS DAC is generating a single 1 GHz tone using a linear laboratory power supply with a 1. 4 MHz 100 mV interferer.

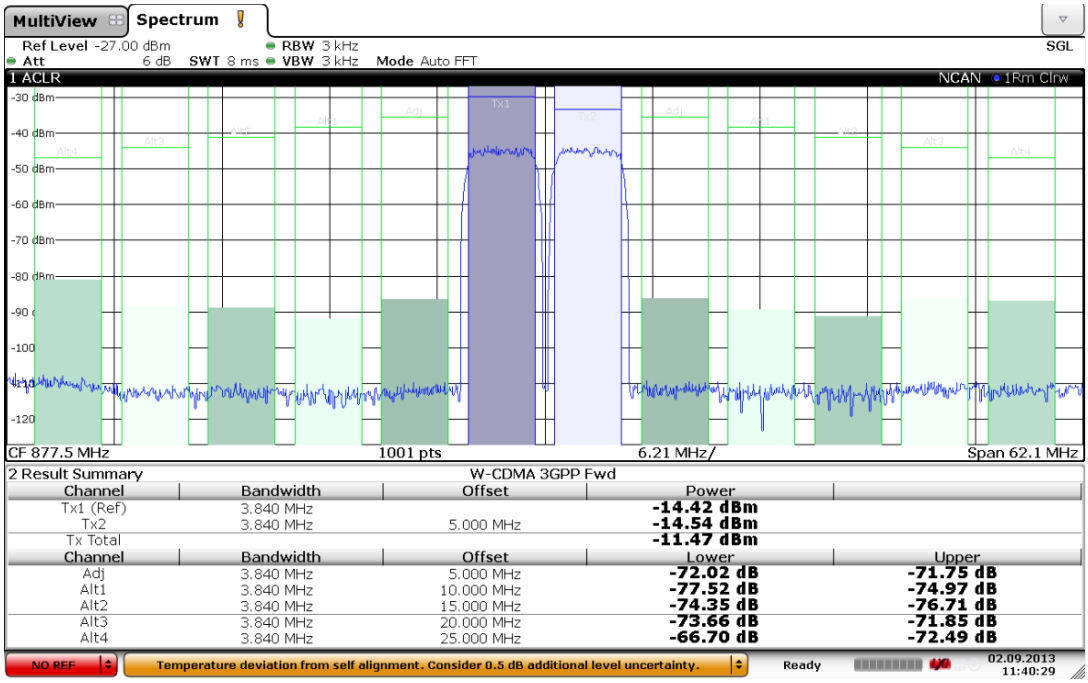


Figure 3-29 Dual carrier WCDMA at 877.5 MHz using a linear laboratory supply for -1.5 V Vss.

Figure 3-30 Dual carrier WCDMA at 877.5 MHz, using a linear laboratory supply for -1.5 V Vss + 100mV 1.4 MHz.

In the second test, a dual carrier WCDMA signal was synthesised using the DAC. Figure 3-29 shows the spectral output when a clean linear laboratory supply is used. The noise floor is located 65 dB below the carriers. Figure 3-30 shows the spectral output when a 1.4 MHz, 100 mV p-p interferer is added to the power supply. An artefact then appears either side of the carriers at a level 20 dB above the noise floor. Thus there is a net loss of 20dB of dynamic range resulting from the 100mV interferer on the power supply in this second application of the same device, compared to a 47 dB loss in Figure 3-28.

3.5 Operational amplifier sensitivity to power-supply noise

Dominant pole compensation is used in operational amplifiers design to force the gain to drop to less than unity before the various combined poles result in a 180 degrees total phase delay. That intentional first pole is typically placed in the region of several Hertz or hundreds or Hertz in modern operational amplifiers [29]. If, as is likely, the noise path for power supply interferers is before that dominant pole in the operational amplifiers circuit, then the ability of the operational amplifier to reject such interferers falls with the decay rate of the dominant pole. A plot of AC PSRR of a typical operational amplifier corresponds to a signal path frequency plot of the same device. The pole in the AC PSRR will be seen as the signal path dominant pole.

A modern operational amplifier designed for low,-noise, low-distortion on a BiCMOS process was chosen to characterise for AC PSRR. Figure 3-31 shows the AC PSRR plot. The dominant pole is seen below 1 kHz. At 1 MHz, where power supply ripple would typically be found as outlined in Chapter 2, the amplifier rejection is now down to approximately 30dB [29]

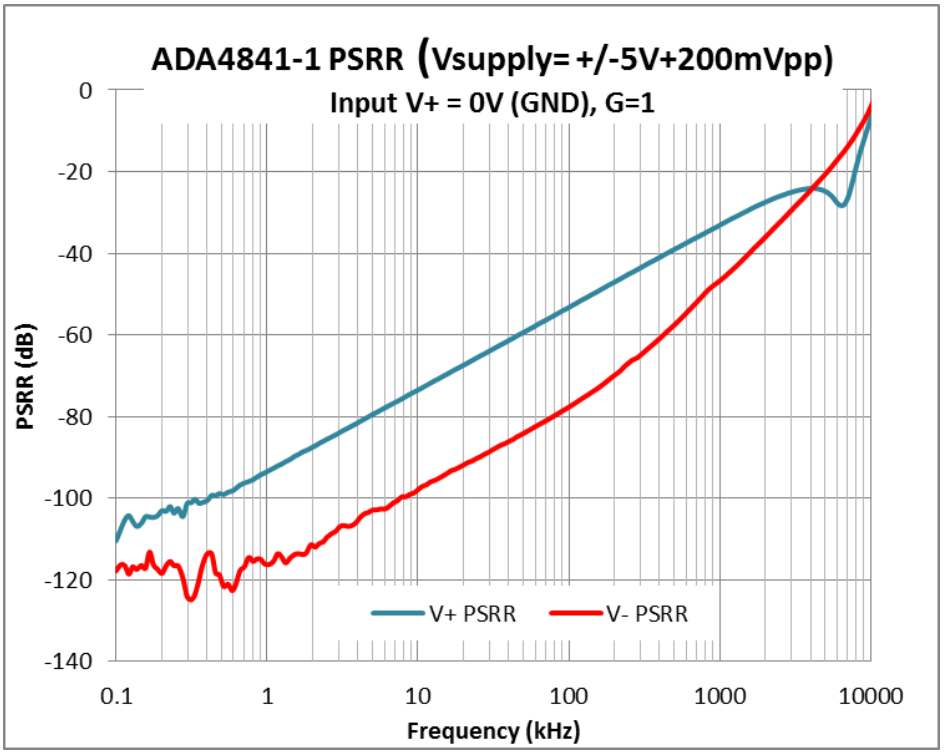


Figure 3-31 A BiCMOS Operational amplifier AC PSRR [30]

3.6 PLL sensitivity to power-supply noise

Figure 3-32 shows a representative modern frequency synthesiser. It comprises an integrated VCO, fractional-N and Integer-N PLL. It is used to synthesise RF carriers from 138 MHz to 4.4 GHz. The sensitivity of these devices to broadband noise as characterised by phase noise and jitter has been presented elsewhere [20]. This study focuses on the carrier intermodulation that is seen to result from a single dominant interferer presented on the power supply pin of the synthesiser under test.

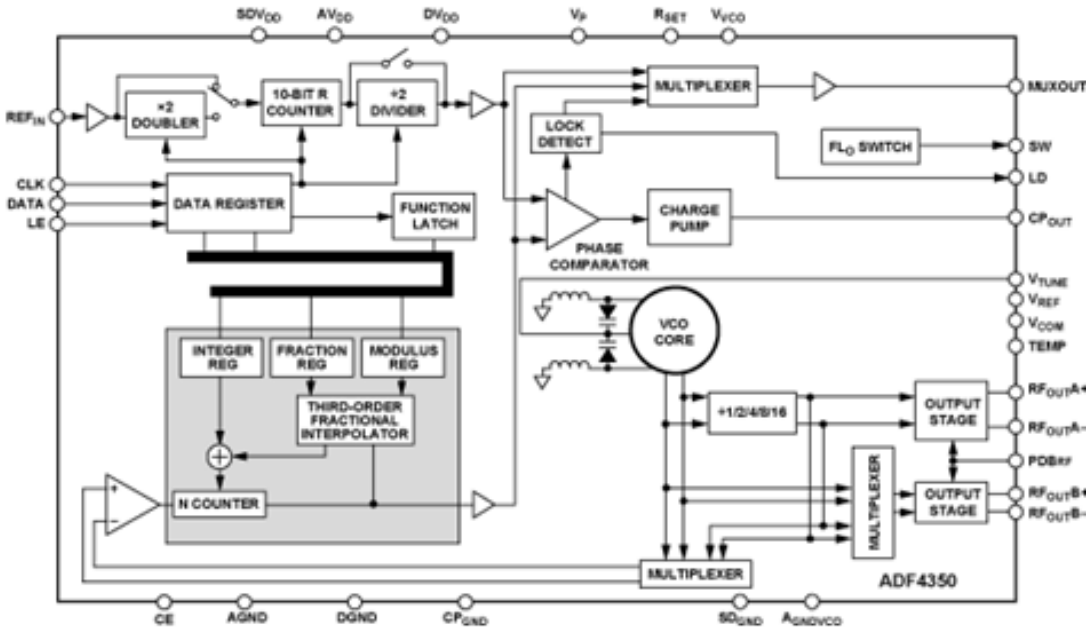


Figure 3-32 A modern frequency synthesizer with integrated VCO [31]

A block diagram of the test setup used to characterise the effect of power-supply noise on a frequency synthesiser is shown in Figure 3-33. A 1mV RMS signal at 20 kHz, 100 kHz, 1 MHz test frequencies respectively were injected onto the power supply while the synthesiser was generating a 4.4 GHz desired output tone.

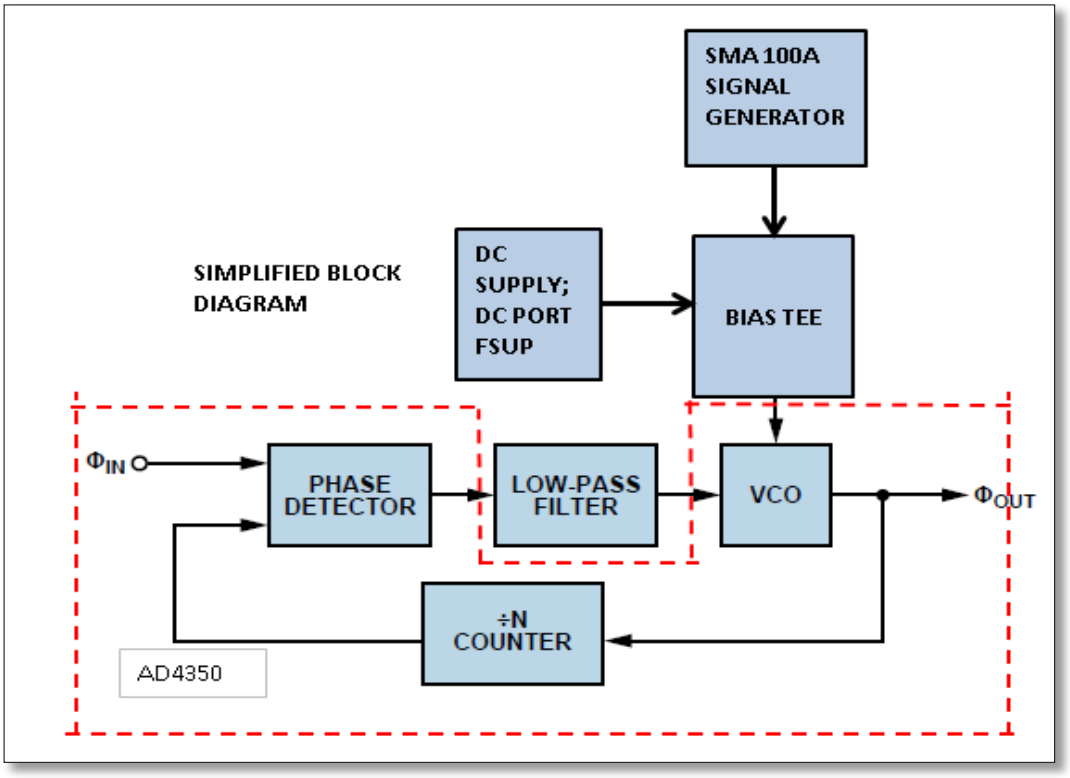


Figure 3-33 Generic frequency synthesizer power-supply noise test setup using Rhode & Shwarz SMA 100A signal generator

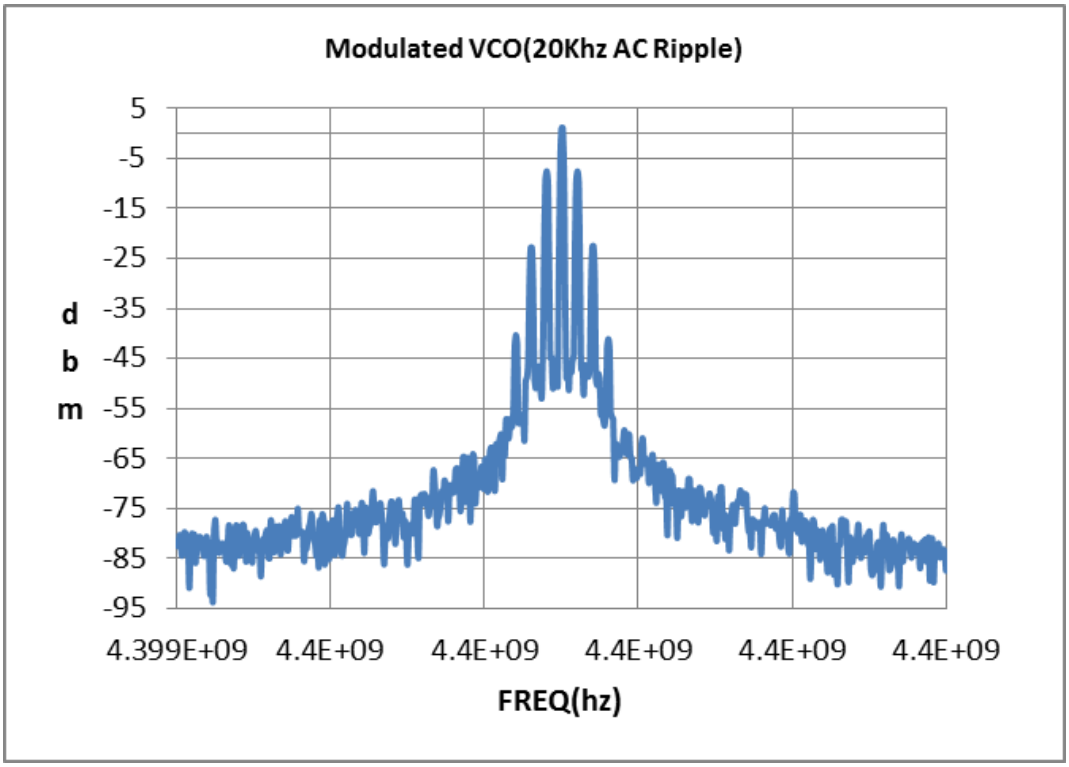


Figure 3-34 Synthesizer tested with a 20 kHz supply interferer

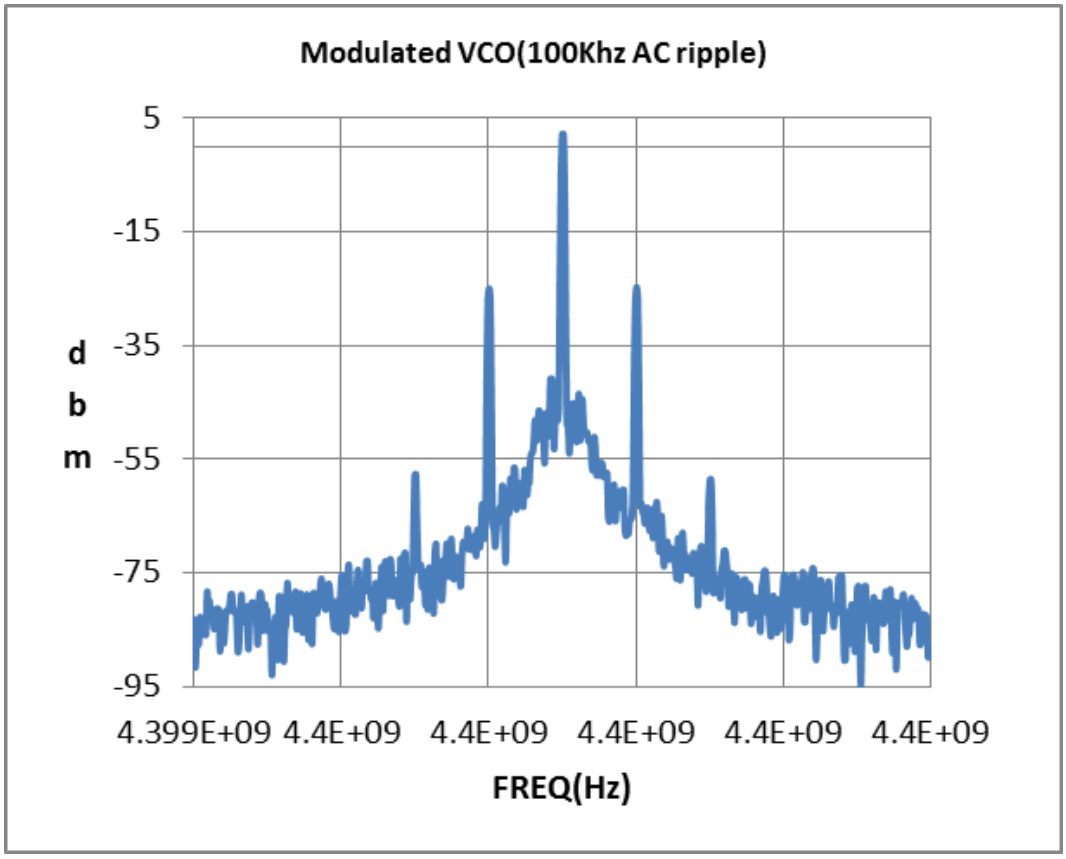


Figure 3-35 Synthesizer tested with a 100 kHz supply interferer

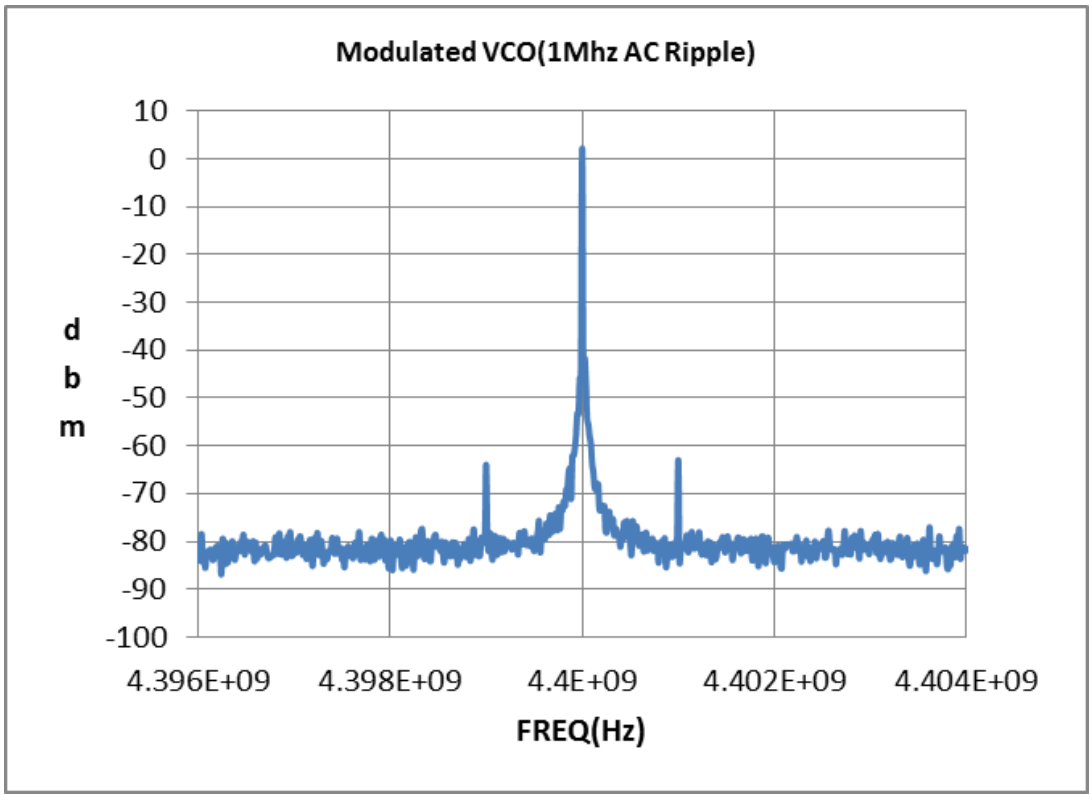


Figure 3-36 Synthesizer tested with a 1 MHz supply interfered

Figure 3-34, Figure 3-35, and Figure 3-36 show the output spectrum seen from this frequency synthesiser when a 1 mV RMS tone was coupled onto a linear laboratory supply. The resultant frequency modulation of the desired 4.4 GHz output shows a 40 dB / decade decline in magnitude with increasing test tone frequency. This is consistent with the expected modulation index change associated with narrow band frequency modulation [32]. It suggests that near-DC power supply interferers are more harmful to this class of frequency synthesiser than the higher power supply ripple frequencies outlined in Chapter 2. This is the opposite case to that outlined for data converters and operational amplifiers in sections 3.3, 3.4 and 3.5.

3.7 Chapter summary

This chapter presented the experimental results seen when an AC test tone was added to the power supply of representative modern data converters, operational amplifiers and frequency synthesisers. The frequencies used were based on the results presented in Chapter 2 where the frequencies generated by typical switch mode power supplies were examined. The data presented in this chapter suggests than a method which focusses on notching out the ripple generated by the switch-mode power supply would be sufficient to allow most data converters and operational amplifiers to achieve optimal performance. These devices have sufficient AC PSRR at frequencies below the ripple fundamental to remain unaffected by white, control loop and other noise presented by the power supply below its ripple frequency. The balance of this report will explore novel ways to notch out and suppress switching regulator noise.

Chapter 4 Use of a track and hold on an ADC power supply to reduce ripple susceptibility.

This chapter presents the results of testing a totally novel proposed solution that can be applied to ADCs in the event that the conversion time allows sufficient time to operate an added isolation switch on the power supply. A proposed technique will be presented here that tracks and holds the power supply during the sensitive part of the total conversion time and only recharges from the noisy power supply during the insensitive time. Sinc function (i.e.Sin(x)/x) attenuation of the power supply ripple resulting from the track and hold operation will be tested as a novel technique to effectively filter and transpose the ripple to a less harmful frequency.

4.1 The hypothesis.

It was highlighted in section 3.3.1 that a SAR ADC architecture has a total conversion time composed of two distinct phases, a differential signal acquisition time and a single-ended bit-trials time. To a first approximation, it is hypothesised that the power supply could be isolated during the sensitive bit-trials time. If the supplies to the sensitive analog circuitry were isolated from the insensitive circuitry then an isolating switch (a “supply-sampling” switch) could be used to power the sensitive circuitry from the decoupling capacitor (“supply-sampling” capacitor) alone. This concept is shown in Figure 4-1. The sensitive circuitry would comprise the internal DAC switches, reference, preamplifiers and comparator. The insensitive circuitry would comprise the timing and all digital circuits including any time subsequent to the bit-trials when redundancy techniques are used to digitally construct the output code.

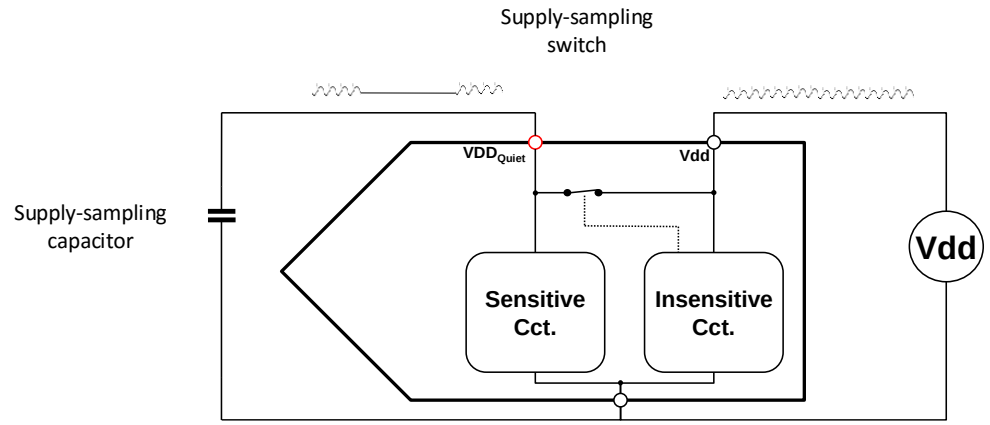


Figure 4-1 Basic concept of track and hold for power supply to sensitive circuitry in ADC

This technique is novel. A patent (US 8975953) has been granted to the authors on the concept, as an outcome of this project.

A deeper review reveals that the supply-sampling capacitor doesn't fully isolate the sensitive circuitry from the supply ripple. There is a track and hold action whereby the ripple is sampled onto the supply-sampling capacitor. So not only will the ripple occur at its original frequency but it will also appear at sum and difference frequencies either side of the conversion frequency and its integer multiples, in a sinc function decaying pattern because of hold taking place in the time domain [33]. The ratio of Fripple to Fconversion for the track and hold determines the magnitude of the original and aliased components. In this case, the hold time is the "supply-sampling" time. It is proposed that use can be made of the sinc function low pass filtering effect as Fripple increases relative to Fconvert when the samples are converted and viewed in the continuous domain over many conversions. Critical to achieve the sinc function advantage, the sensitive circuitry only sees the sampled waveform during the hold time. As the ripple frequency increases into the zone of decreasing native AC PSRR of the ADC, the increased attenuation to the fundamental resulting from the sinc function sampling attenuation effect will cause the ripple to be less harmful. As that

happens, an increasing magnitude aliased (Fconvert-Fripple) component occurs are a lower frequency, where the ADC has increased native AC PSRR to attenuate this secondary, aliased component as seen in Figure 3-7. For this proposed technique to be effective, the ADC conversion rate needs to be in the same frequency order of magnitude as the ripple frequency. Sinc function attenuation only becomes significant when the sampled frequency is greater than half the sampling frequency, as shown in Figure 4-2.

4.2 A track and hold in the frequency domain.

To understand why a track and hold on the power supply of a mixed-signal load can reduce the effect of power supply ripple it is useful to review what happens to the frequency spectra in a track and hold operation. For this section the term Fsample is being used to replace Fconversion for the sampling frequency, and Fin interchanges with Fripple for the frequency being sampled, as the explanations hold for a track and hold operation that is a generic and may not necessarily be followed by an ADC. A track and hold or sample and hold differ from pure discrete sampling in that a

Sin (x) / x, (where $x = \pi Fin/Fs$), low pass filtering effect on the signal being sampled occurs as a result of the zero-order hold [34].

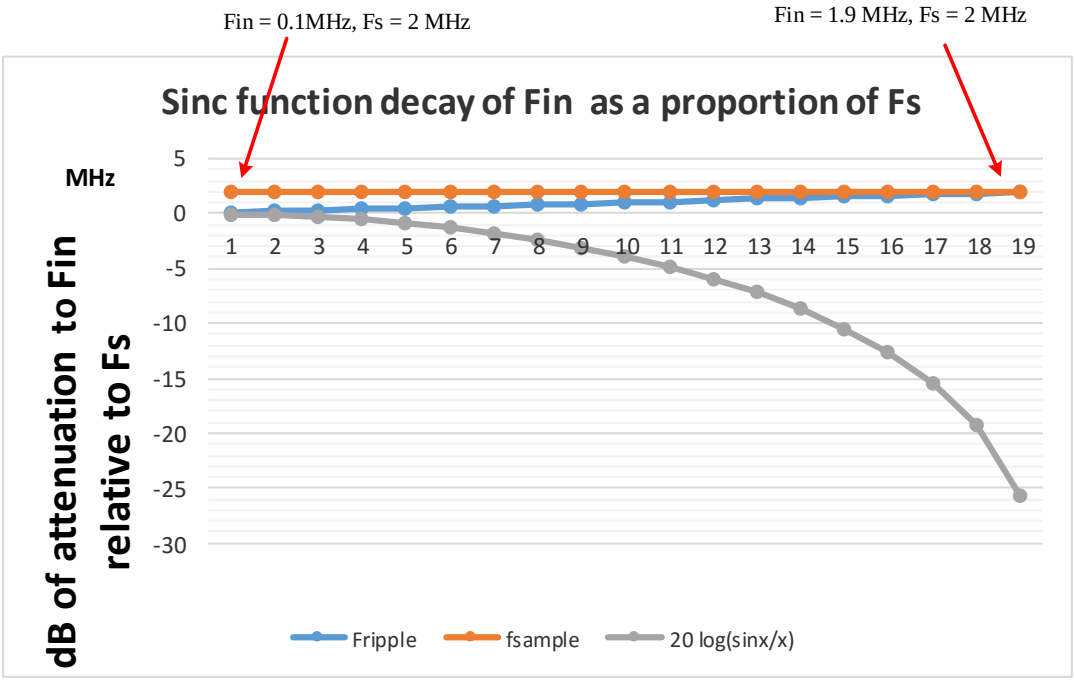


Figure 4-2 Sinc function attenuation of sampled signals depends on their frequency relative to the sampling frequency

Figure 4-2 shows a plot showing Fripple (blue) as an increasing ratio of Fsample (orange) and the resulting attenuation (grey) of Fin relative to Fsample as calculated by Equation 4. The attenuation caused by the sinc function reaches 26dB when Fin = 1.9Fs.

$$Fin\ mag.\ ratio = (Sin\left(\frac{\pi Fin}{Fs}\right))/(\frac{\pi Fin}{Fs}) \qquad \text{Equation 4}$$

Simulation

A simulation model of a track and hold was developed using the openly available simulation tool, ADIsimPe, which is based on SIMetrix/Simplis. [9]

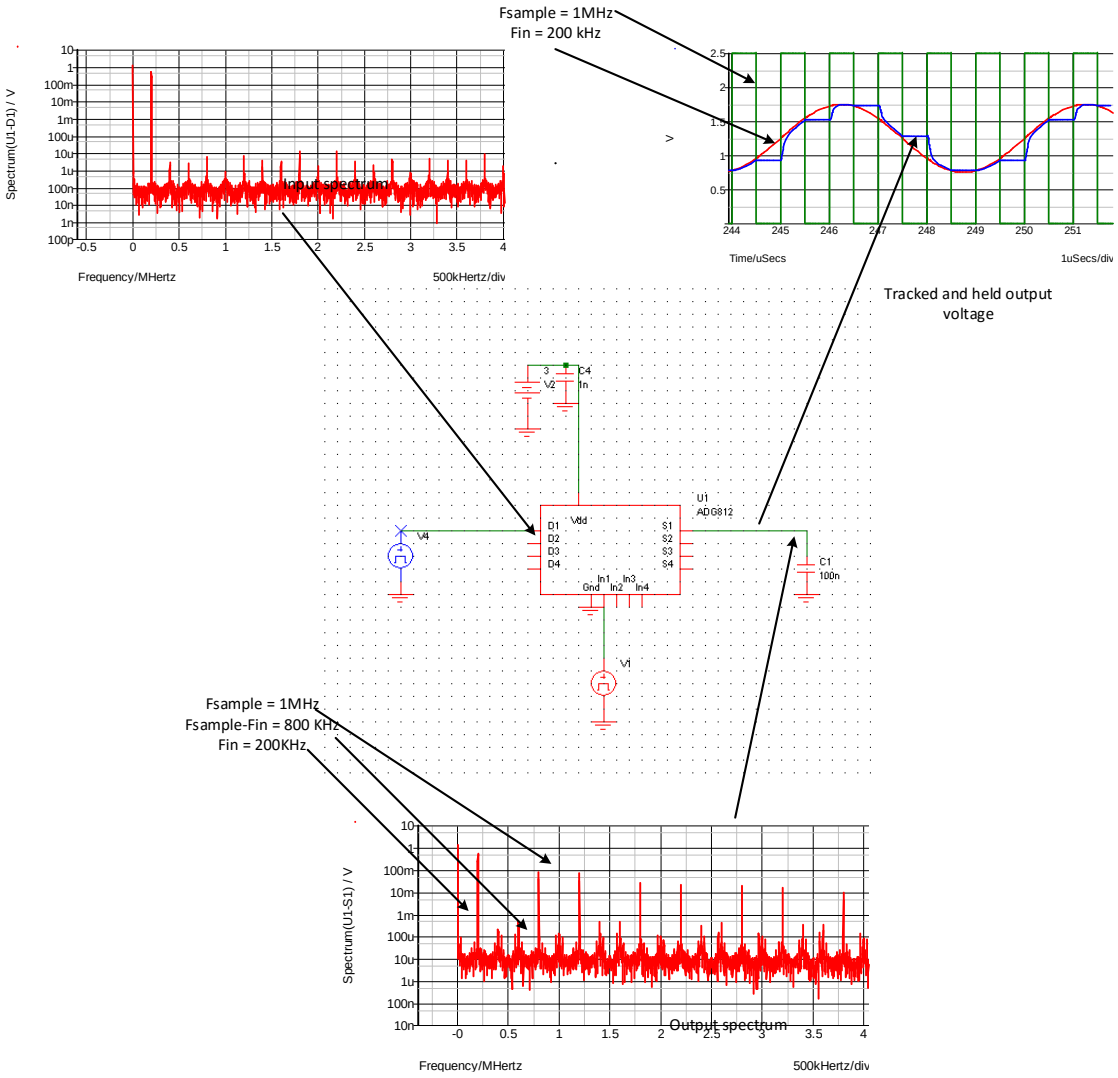


Figure 4-3 Simulated view of basic track and hold operation

The various simulated frequency domain and time domain waveforms of a track and hold are shown in Figure 4-3. It is a basic circuit with a 100 nF hold capacitor, and an ADG812 switch that has 500 mΩ on-resistance [35]. A smaller hold capacitor will lessen the relative effect of the switch on resistance but will increase the droop of the

DC voltage during the bit trials time. The drive signal to the switch is a 3V 50% duty cycle square wave and the input is a pure sine wave with care taken to stay within the specified switch input common mode range. The input signal is seen at its original location but is also aliased to integer multiples of Fsample +/- Fin

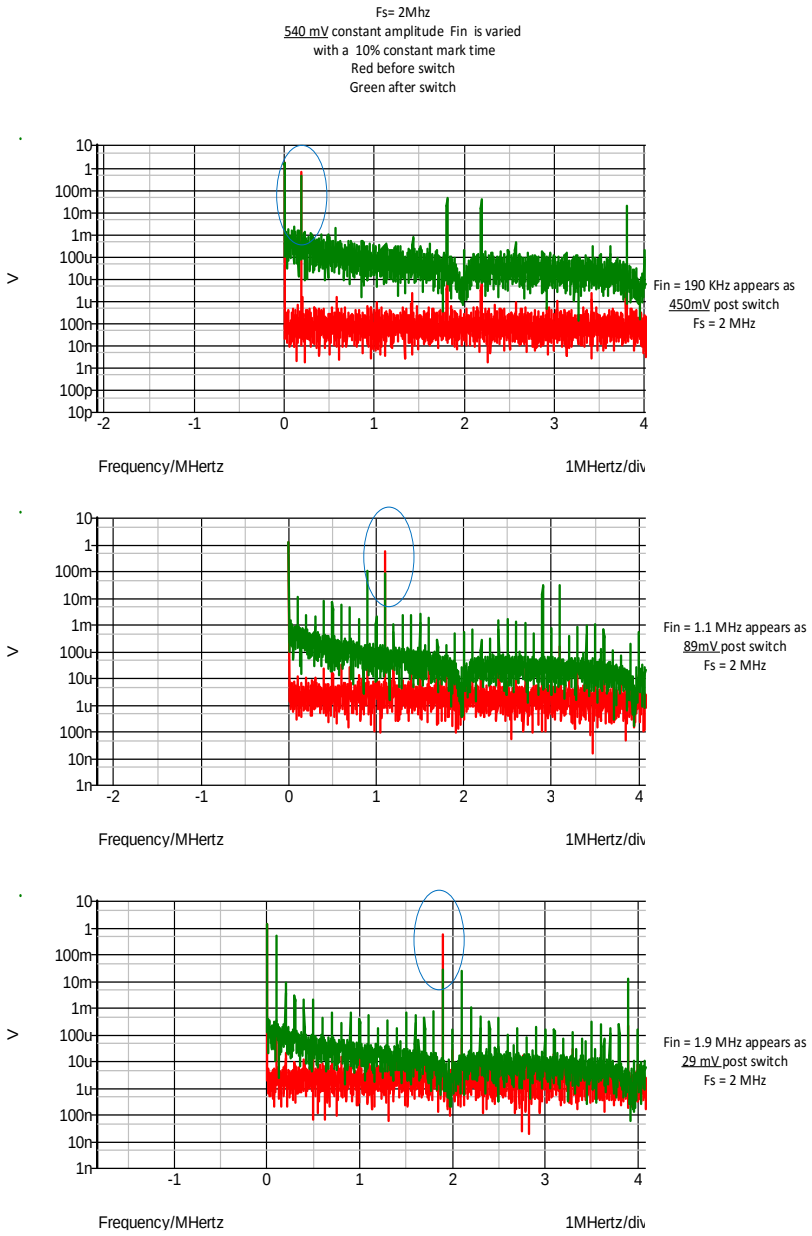


Figure 4-4 Simulated view of the effect of sinc function attenuation of Fin relative to Fsample, as Fin increases relative to Fsample in a track and hold.

As was shown in Figure 4-2 and Equation 4, the output amplitude of the signal being sampled, Fin, will appear at increasingly lower amplitude as its frequency increases relative to the sampling frequency, Fsample. The aliases of Fin that are located at lower frequencies may have a higher amplitude than the original sampled Fin. Figure 4-4 shows a simulated example that demonstrates this concept. As a constant amplitude (540 mV) tracked and held signal, Fin, is stepped from 190 kHz, to 1.1 MHz to 1.9 MHz, with a constant amplitude and an Fsample frequency of 2 MHz, the resulting sample of Fin appears as a 450mV, then 89mV then 29mV output amplitude signal at its original frequency. The simulation is displaying sinc function attenuation. The importance of this concept is that it allows a power supply ripple fundamental frequency to be attenuated at its original frequency, if it is of a frequency close to the conversion rate of the ADC. The aliases of the ripple frequency that reside at lower frequencies than the ripple fundamental may have higher amplitude than that seen at the actual ripple frequency but they will alias to a lower frequency where the ADC has a higher native AC PSRR. Figure 4-5 shows the simulated time domain waveforms corresponding to both the 190 kHz and the 1.9 MHz cases from Figure 4-4. Red shows the sampling waveform, green is the input signal being sampled and blue is the voltage seen on the hold capacitor. It can be visualized from this diagram that a lower frequency alias of the 1.9 MHz input signal is where more energy lies than at the original frequency.

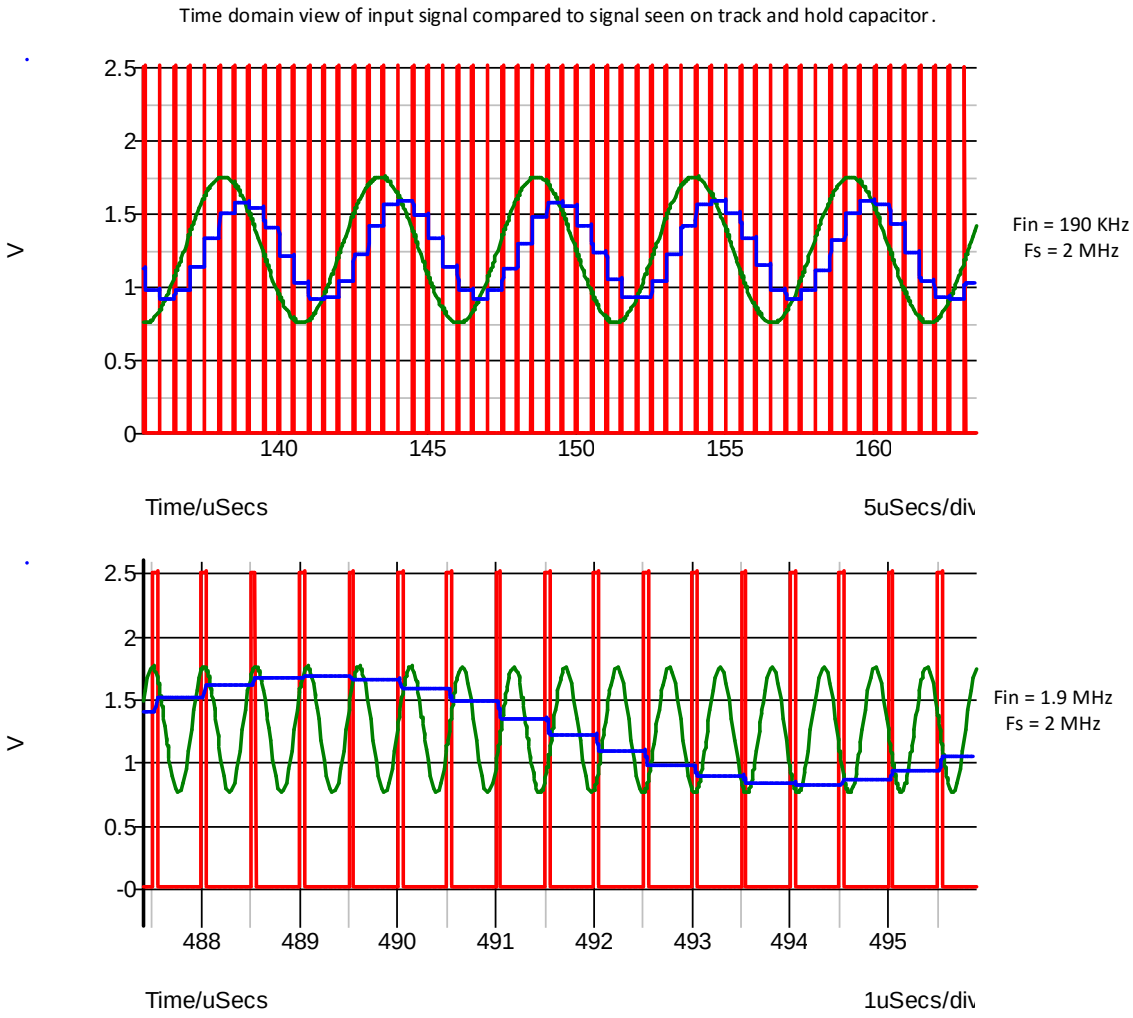


Figure 4-5 Simulated view of time domain waveforms showing the effect of sinc function reduction in the amplitude of Fin post-sampling in a track and hold.

4.2.1 **The effect of the track to hold time ratio.**

Zero crossings in the sinc function envelope occur when Fin = Fs for a true zero order hold. When the hold time is less than 100% of the total sample time, the location of the zero crossings is scaled accordingly [34]. For example a 50% hold time will cause the first zero in the sinc function envelope to occur at 2Fs, as indicated by Equation 5.

$$1st\ Zero\ crossing\ when\ Fin = Fs(\frac{Ts\ total}{Thold}) \qquad \text{Equation 5}$$

As described in [36], a continuous time spectrum analyser measurement reproduces the entire spectrum of the waveform seen on the sampling capacitor but the spectral content of just the held samples is required for proper measurement of the spectra seen by the modified ADC that samples at a time instant within the held waveform.

The significance of this is that the ratio of the total sample time to hold time does not matter to the use of sinc function attenuation of ripple in this experiment. That is provided the following "ideal" conditions exist:

1. There is zero coupling from the insensitive to sensitive power islands.
2. There is zero sensitivity to power supply ripple in the sensitive circuitry during the insensitive time.
3. There is zero feedthrough on the supply-sampling switch.

   The effect of violating any of these three conditions will be to allow some ripple feedthrough and cause the zero crossings in the sinc function to shift to a higher frequency than Fs, giving less attenuation on the ripple signal than predicted by Equation 4.

4.2.2 **Physical measurement**

Figure 4-6 shows measured spectral plot of the result from a 91 kHz signal being sampled at 2 MHz using the sampling-switch setup. Two plots are shown in this diagram. The red trace was taken by shorting out the sampling switch, for comparison purposes.

Figure 4-6 Measured spectral content on AVdd following the action of a track and hold on that supply.

4.3 Modification to the SAR ADC to accommodate the supply-sampling switch

The PMOS switch used requires in the region of 10 nS turn on time with a 35 pF load. The 16 bit SAR ADC used in Figure 3-7 was chosen as one of the test architectures because the 1 MHz conversion frequency corresponding to a 1 µS total conversion time allows adequate time to operate the FET switch, unlike the pipelined ADC in Figure 3-9 which has an 8 nS total conversion time. A suitable sigma-delta ADC was also modified and tested to verify the hypothesis regarding the possible benefits.

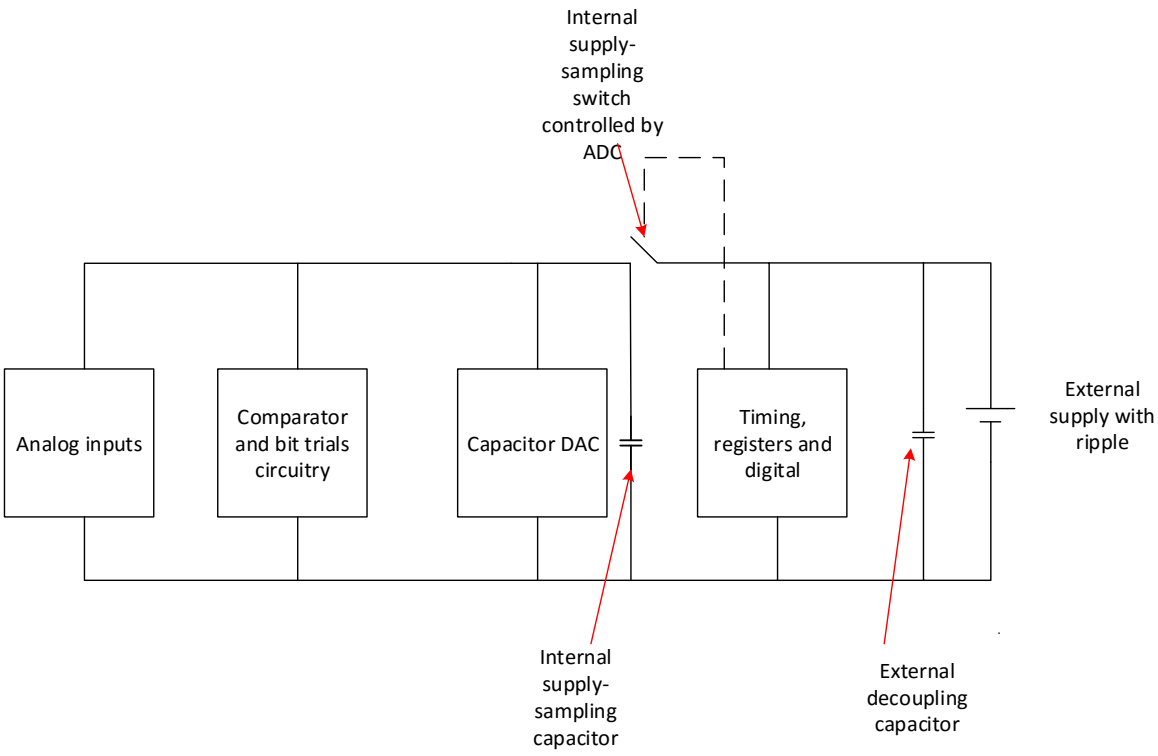


Figure 4-7 ADC blocks powered from sensitive and from insensitive supplies.

A plan of the ADC blocks predicted as being less sensitive to power supply ripple is shown in Figure 4-7. Essentially it is all the digital and timing blocks that are forecast as likely to be insensitive. The sensitivity exhibited by the timing blocks would result in aperture jitter that results in spectral spreading of the fundamental across FFT bins, but not an increase in the specific power supply ripple magnitude spectral bins [1]. A large 3800µm/0.24µm (W/L) PMOS device was used as the switch as it was desirable to reduce the on resistance as much as possible, to prevent the RC filter benefit effect masking any frequency mapping benefit. This device has a 500 mΩ on resistance. The signal used to drive the switch was the "Start of Bit Trials" signal. Figure 4-9 shows the circuit location of the switch and driving inverter. An ADICE (proprietary Analog Devices Integrated Circuit Emulator Spice based simulation tool) simulation showing the timing involved is shown in Figure 4-8.

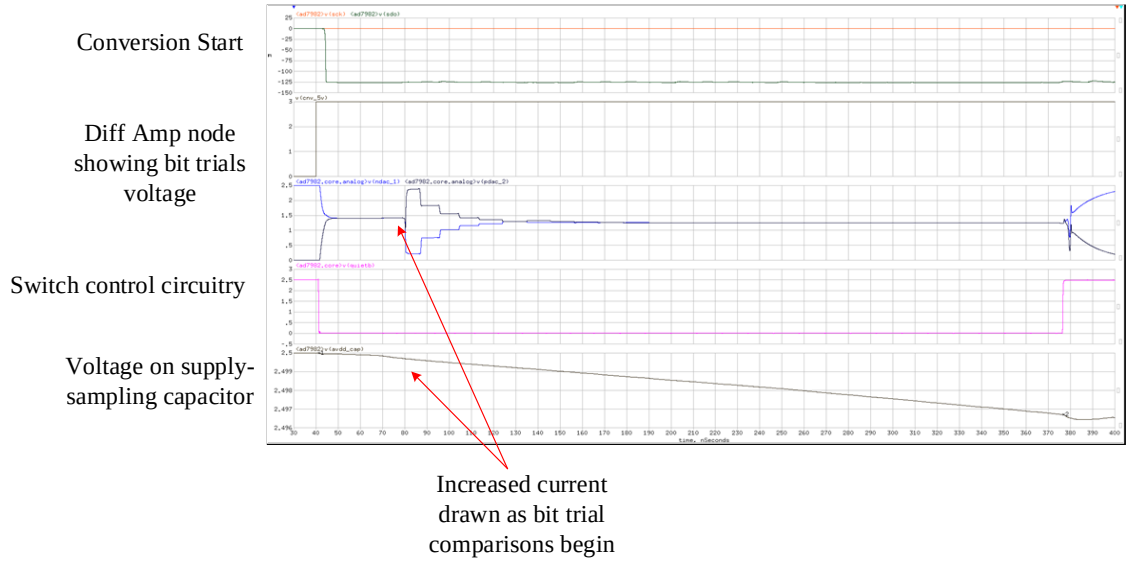


Figure 4-8 Simulated timing for power supply supply-sampling switch.

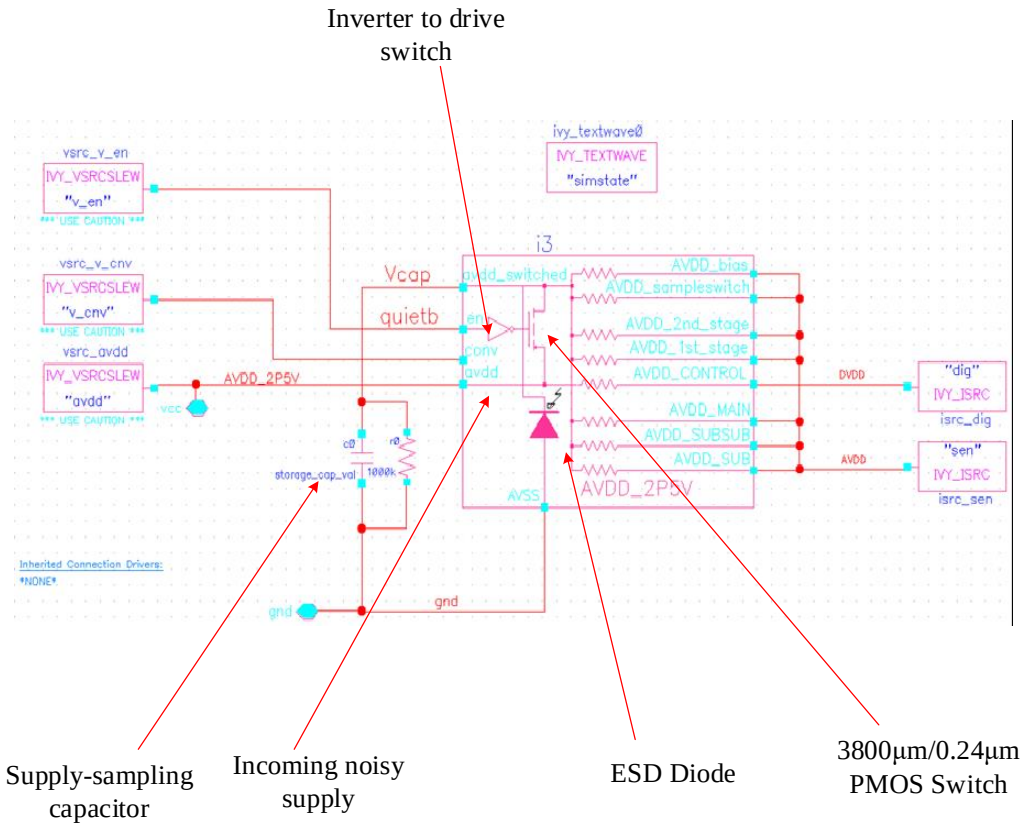
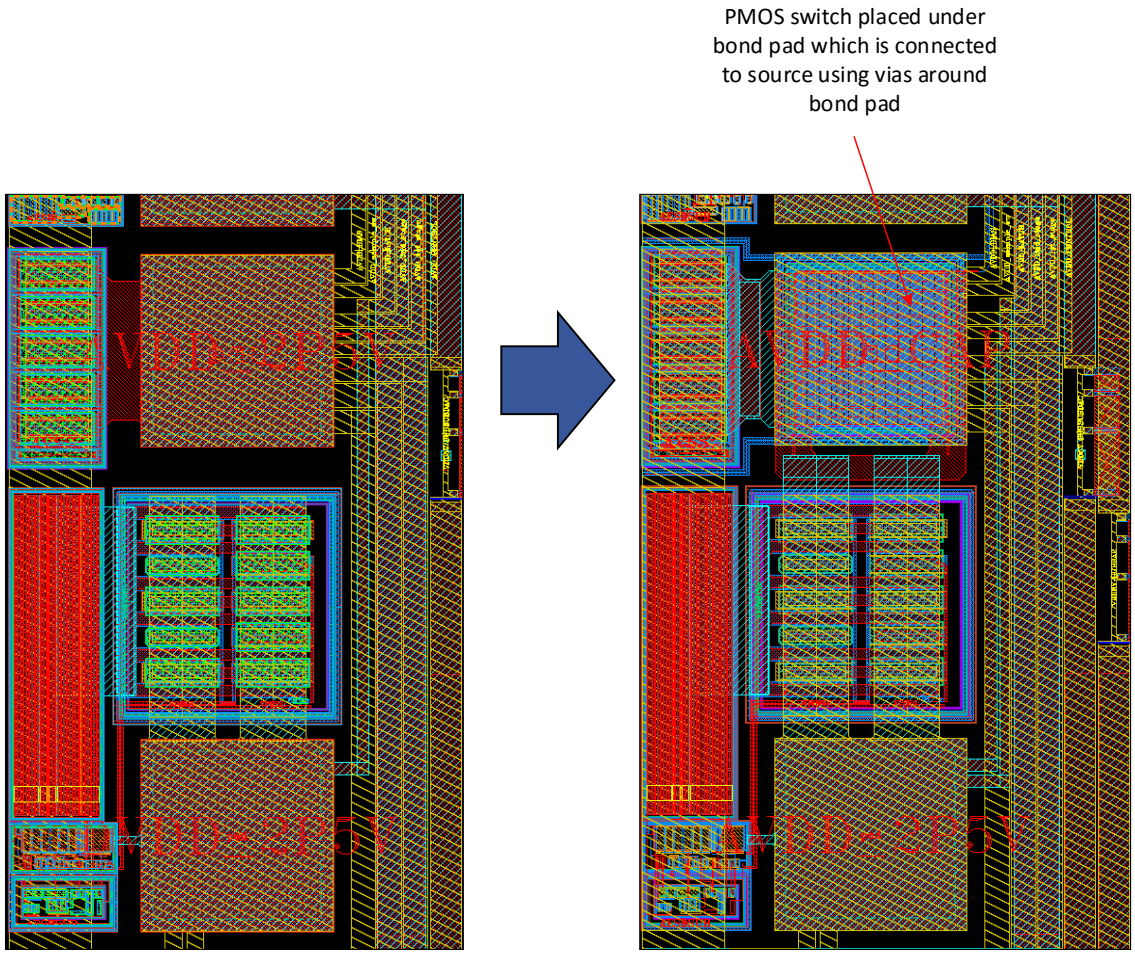


Figure 4-9 Circuit location of the supply-sampling switch

For the initial circuit build, the supply-sampling capacitor was left off-die with the supply-sampling switch integrated on-die. There was adequate room underneath an existing bond pad to fit the PMOS device as shown in Figure 4-10. The required inverter is shown in Figure 4-11. The modified scheme to give a free bond pad for the external supply-sampling capacitor is shown in Figure 4-12.



Before modification

After modification

Figure 4-10 PMOS supply-sampling switch placed under bond pad

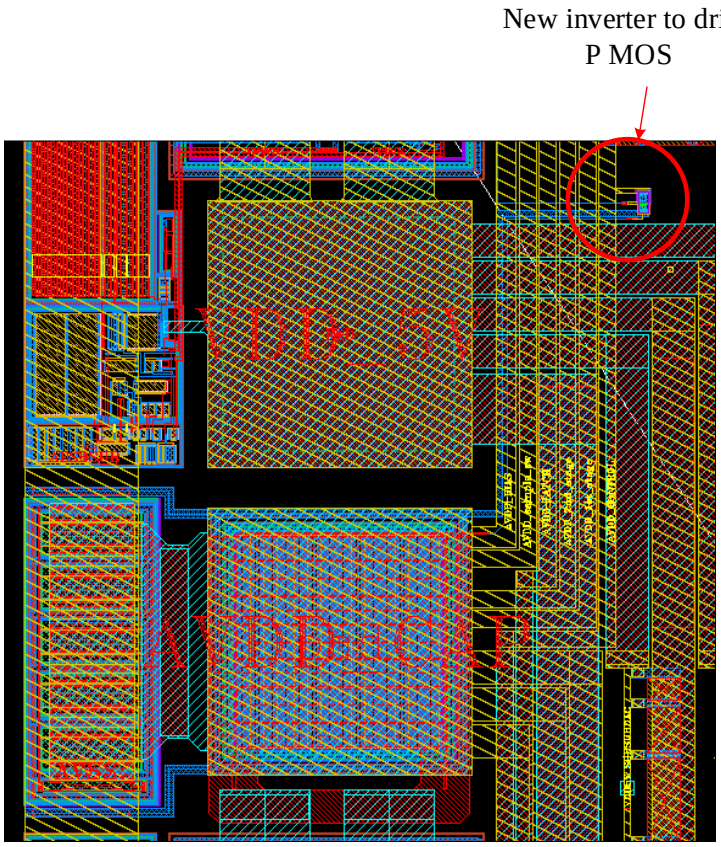


Figure 4-11 Added inverter to drive the supply-sampling switch

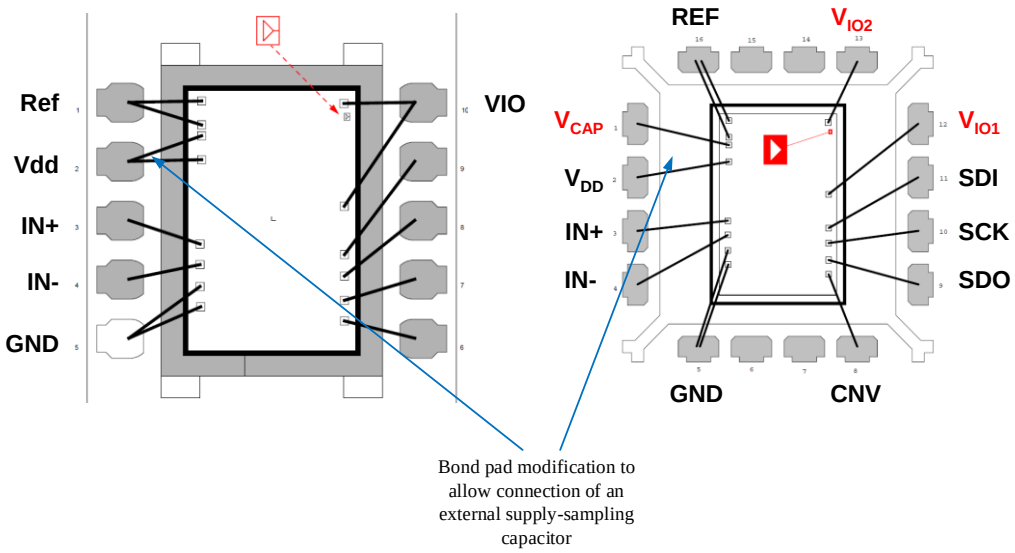


Figure 4-12 Bond pad and lead frame changes to allow external supply-sampling capacitor

4.3.1 **Results obtained from the modified SAR ADC.**

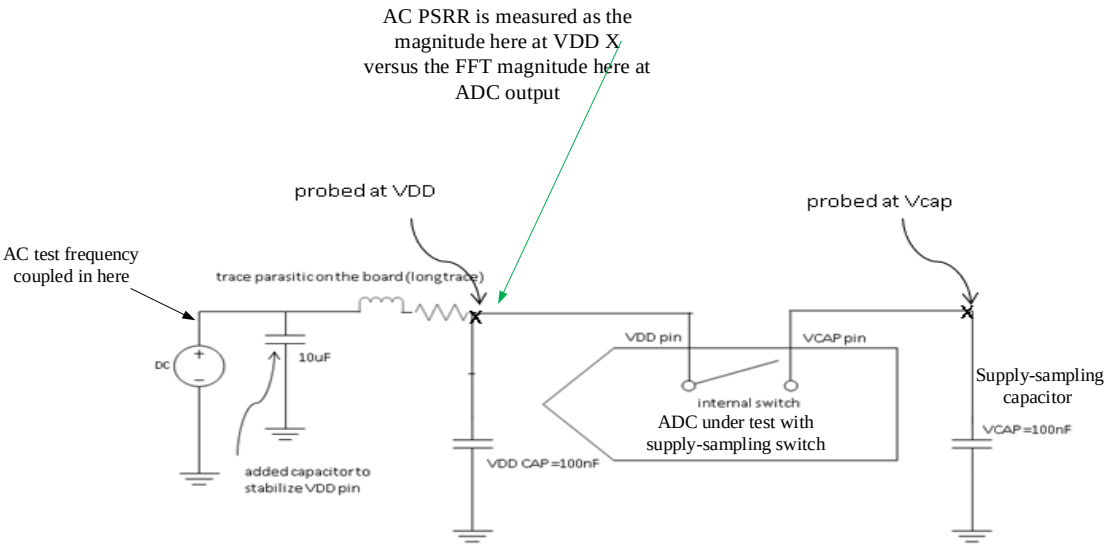


Figure 4-13 Test setup for SAR ADC supply-sampling switch

The test setup used to test the modified SAR ADC is shown in Figure 4-13. The conversion frequency was 1 MHz. The AC source was buffered with an AD817 operational amplifier [37] in unity gain configuration, to prevent the output impedance of the AC source having an attenuation effect in concert with the supply-sampling capacitor. Figure 4-14 shows a oscilloscope picture of the various signals from the test setup from the case of a 332 kHz ripple signal and a 1 µs. conversion time.

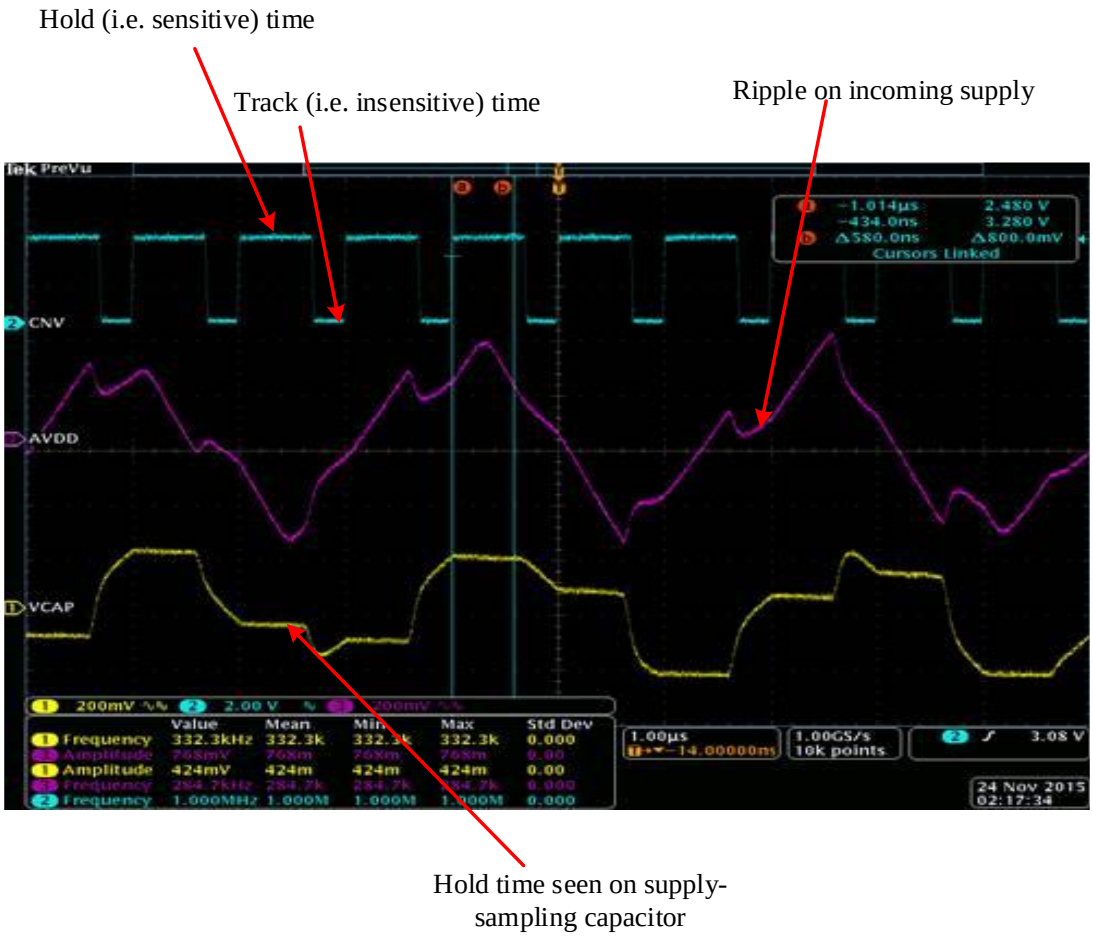


Figure 4-14 Oscilloscope traces of various signals from modified SAR ADC test setup

For this test, AC PSRR is defined as the ratio of the AC test frequency magnitude at the device Vdd pin to the magnitude of that frequency seen at the ADC output using an FFT.

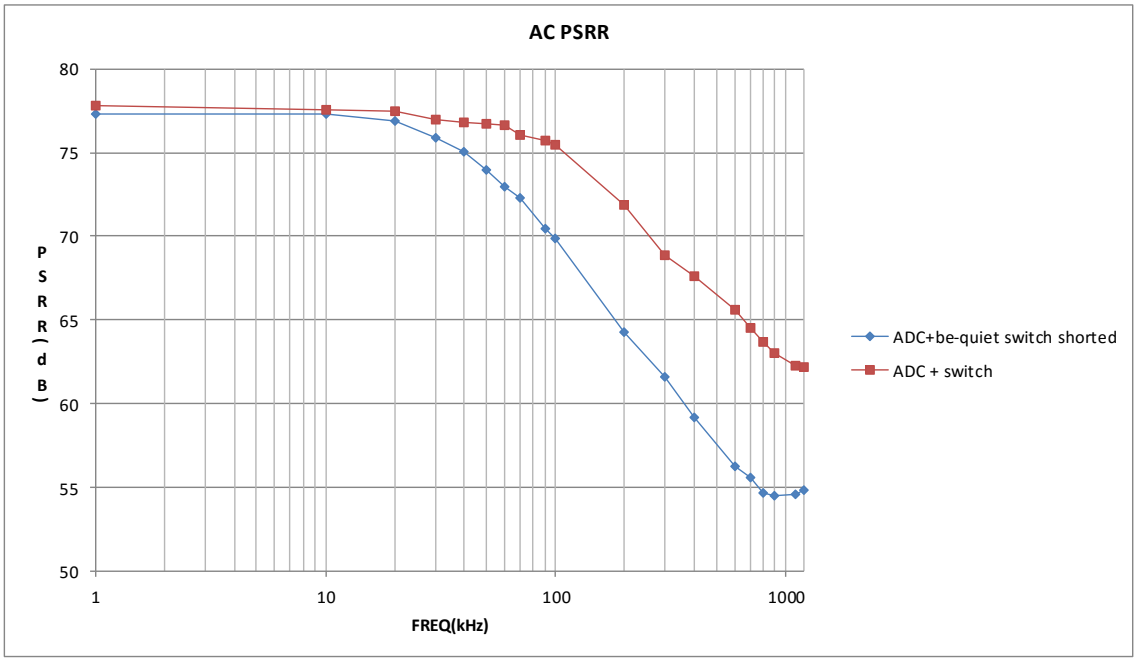


Figure 4-15 AC PSRR results from SAR ADC with no supply-sampling switch versus the same ADC with a supply-sampling switch fitted.

The results obtained are shown in Figure 4-15. The addition of the supply-sampling switch alone improves the AC PSRR (red line versus blue line) by an increasing amount as Fripple approaches Fconvert.

4.3.2 **Discussion of results from the modified SAR ADC.**

There were variables in the experiments carried out on both the SAR and sigma-delta ADCs (that follows in the next section).

1. In the case of the sigma-delta ADC examined in section 4.4 there are several sampling events in series. There is the sampling action of the supply-sampling switch, followed by chopped input buffers, then by the ADC modulator, followed by the digital filter. Aliases can end up in many places depending on the relative frequencies of each sampling stage.
2. An assumption was made regarding what circuitry was insensitive and what was sensitive to power supply ripple for both ADC architectures looked at. That assumption was subject to error caused by stray coupling between the two regions.

   With those caveats the following observations can be drawn:

	Ripple attenuation achieved (dB)		
Fripple to Fconvert Ratio	**Predicted by Sinc**	**Simulated track and hold**	**Measured with modified SAR ADC**
10%	0.13	1.58	4
55%	4.8	10	10
95%	25	25	12

Table 2 Comparison of theory, simulation and measured results for supply-sampling switch technique on the SAR ADC

A comparison of the ripple attenuation predicted by the basic theory put forward in Equation 4, a simulation of the track and hold shown in Figure 4-4 and the actual results achieved with a SAR ADC modified to use a supply-sampling capacitor and shown in Figure 4-15 is shown in Table 2. The actual measured values follow the same trend line as the calculated and simulated results but differ by 50% when Fripple was 95% of Fconvert of 10%. As the ripple test frequency is increased parasitic coupling from the insensitive to sensitive islands of the circuitry would have increased and had

the effect of decreasing the sinc function attenuation achieved. In addition, the measurement of improved ripple rejection used here is a relative measurement. It is relative to the AC PSRR measured with the supply-sampling switch shorted. In Figure 4-15 the corresponding measurement shows a corner frequency at 600 kHz and AC-PSRR begins to improve again above that corner frequency. This takes several dB from the relative measurement of the performance with the supply-sampling when compared.

The performance difference seen with and without the sampling switch shorted out can only be caused by two possible phenomena: The sinc function effect as discussed (a) and (b) an increase in series resistance caused by the switch. Everything else was common to both tests.

To rule out the possibility that this ripple-attenuation improvement was caused by straightforward RC filtering of the ripple, a continuous time spectrum analyser was used to measure the average amplitude of the ripple signal at the supply-sampling capacitor both with and without the supply-sampling switch toggling. If the improvement seen in Figure 4-15 was attributable to increased RC filtering caused by the switch resistance, it would display as lower amplitude ripple in this measurement. The measured results are shown in Figure 4-16. The 80 kHz corner was caused by the total decoupling capacitance of approximately 20 μF on the test board. In the area of interest, above 100 kHz, where the two ADC setups show differing results in Figure 4-15, it is seen in Figure 4-16 that the continuous time view shows near identical ripple signal amplitudes. (Note that the measurement used for the AC PSRR plots in this thesis involved measuring the ripple amplitude at the input pin and in the FFT output so the slope seen in this graph is calibrated out). Further, to question if it was the case that the held-sample was itself attenuated by the Ron of the switch in conjunction with

the supply-sampling capacitor during signal acquisition, the corner frequency from a 0.5Ω Ron and a 100 nF supply-sampling capacitor is at 3.18 MHz which beyond the range in use here.

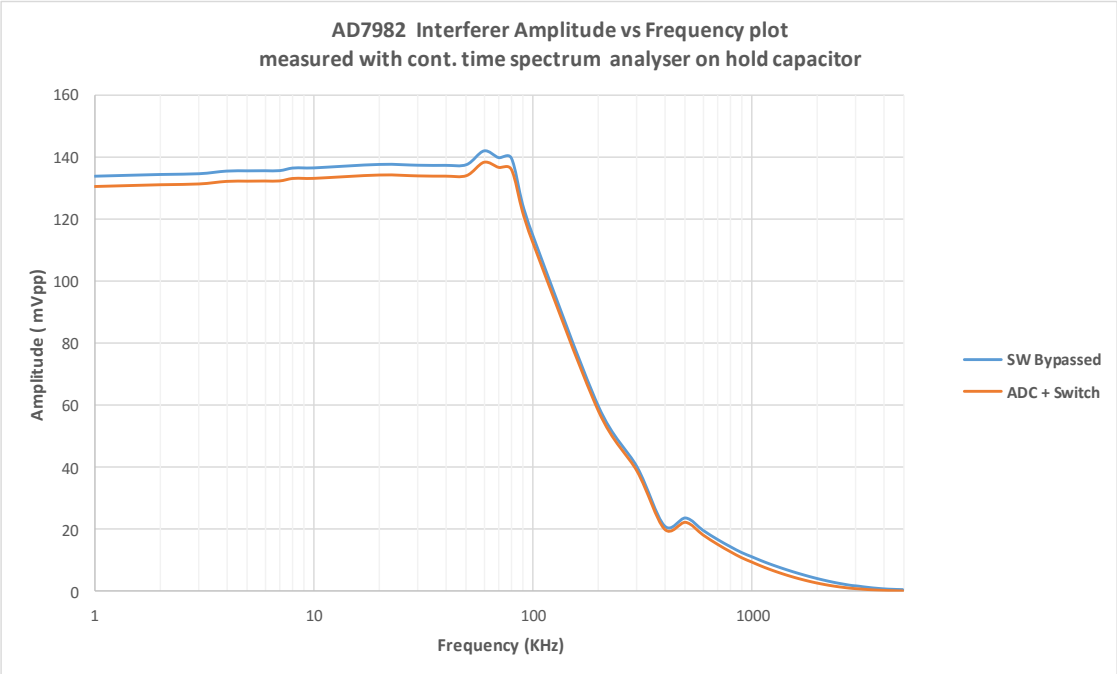


Figure 4-16 Continuous time spectrum analyser view of supply-sampling capacitor with switch operating and bypassed

4.4 Modification to the sigma-delta ADC to accommodate the supply-sampling switch

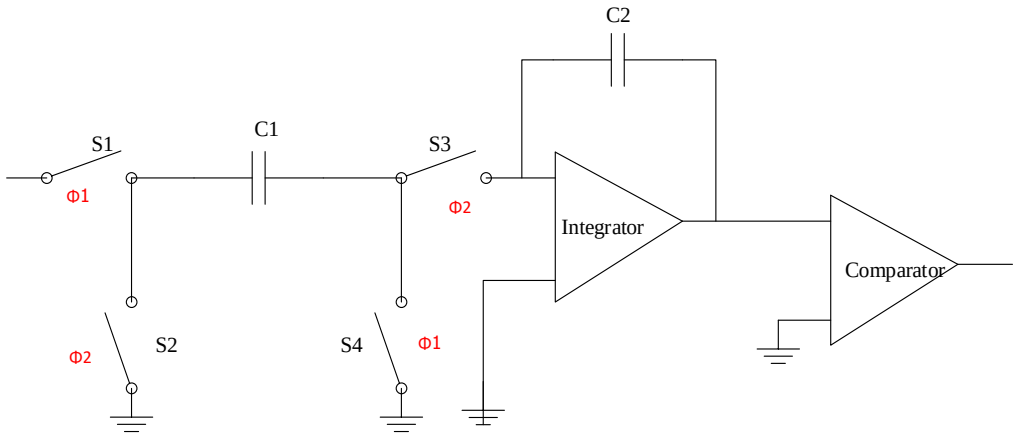


Figure 4-17 Phase timing of switched capacitor integrator

The relative timing of signal acquisition and integration in a switched capacitor first order sigma-delta ADC architecture is shown in Figure 4-17. During Φ1 time, S1 and S4 close while S2 and S3 open. Conversely, during Φ2 time, S2 and S3 are closed and charge is transferred from C1 to C2.

In Φ1 the only path for power supply borne noise to interfere with the signal path would be through on-resistance modulation of S1 and S4. But this would be expected to be a lot less than during Φ2 when power supply borne noise would corrupt the integrator's amplifier. Φ2 is the "supply-sampling" time in this architecture.

The particular 24-bit, 2 MHz sampling, 1 MHz Fmod (2 MHz Fconv.) , 1.8V sigma-delta ADC used was chosen because the layout could easily be modified to allow access to the Φ1 signal external to the ADC, through the Sync/Error pin by means of a metal mask change.

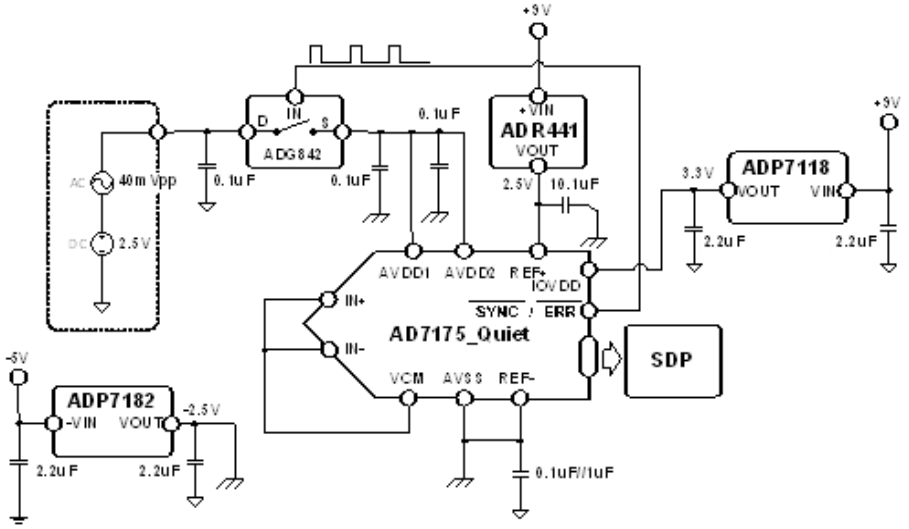


Figure 4-18 Sigma-delta ADC modified for supply-sampling switch

The test setup used to test the Sigma-delta ADC modified for a supply-sampling switch is shown in Figure 4-18. There was insufficient room on the ADC die to incorporate the switch, as had been done with the SAR ADC in section 4.3. Instead, the "supply-sampling" signal was used to drive an external semiconductor switch, the ADG842, as shown in Figure 4-18. The sensitive and insensitive power supplies did not have to be separated. They are already separate on this ADC and labelled AVDD1 and AVDD2 for sensitive supplies and IOVDD for the insensitive supply . For the set of tests carried out, an ADP7182 linear regulator was used to generate a clean, linear supply onto which the test frequency was coupled.

The tests carried out on the modified sigma-delta ADC were:

1. A swept frequency test to investigate if use of the supply-sampling technique contributed frequency zones of the power supply ripple where the ADC performance was improved relative to an unmodified sigma-delta ADC.

The purpose of this test was to examine if the proposed sinc function attenuation improved AC PSRR in the zones either side of the conversion frequency where the sigma-delta architecture is known to be sensitive to power supply ripple.

2. The sigma-delta ADC was powered from an external switching regulator whose clock was synchronized to the supply sampling signal
    a. With the supply-sampling switch operating.
    b. With the supply sampling switch shorted.

    The purpose of this test was to investigate if the supply sampling switch gave any improvement or dis-improvement to the condition where the ripple and conversion frequency were identical frequencies and aliased ripple was anticipated to result in a DC term only. The high resolution of the sigma-delta ADC used provides a useful tool to observe the possible occurrence of other frequencies (such as switch ringing associated with the use of the supply-sampling technique).

4.4.1 **Results obtained from modified the sigma-delta ADC**

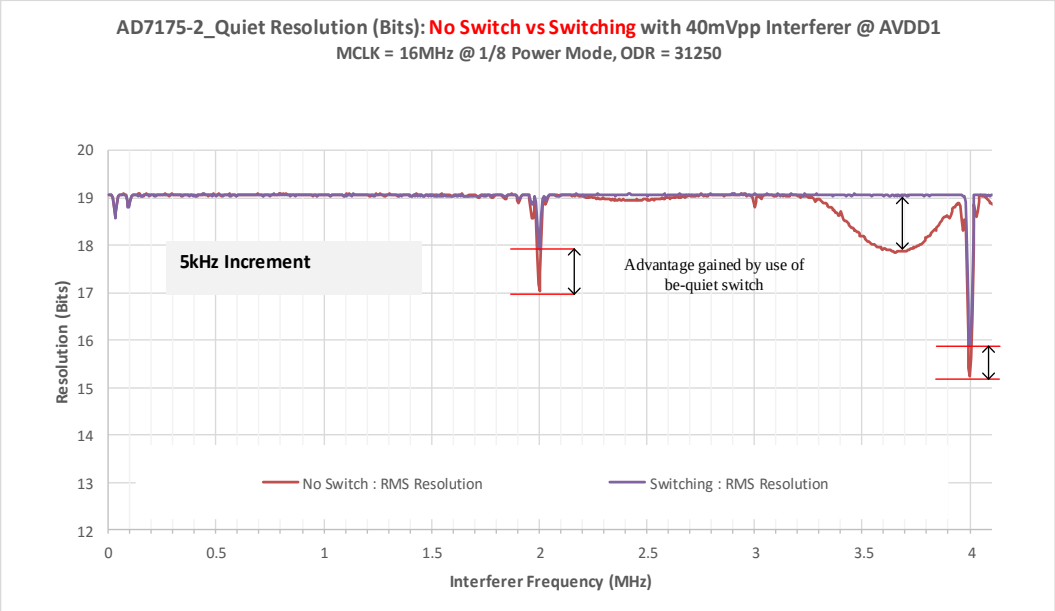


Figure 4-19 Effective resolution of a modified sigma-delta ADC with and without the supply-sampling switch

Modified sigma-delta ADC swept frequency test.

The sigma-delta ADC modified to drive an external supply-sampling switch was tested with a swept power supply interferer. The measured effective resolution (manufacturer specified at 19 bits) was then plotted against interference frequency. Subsequently, the switch was hard wired to be always on and the experiment was repeated. The results are shown in Figure 4-19. A 6 dB improvement from use of the supply-sampling technique compared to the same ADC with the supply-sampling switch shorted, is seen.

The reduction in effective resolution at integer multiples of the 2 MHz clock frequency (Mclock/8) shows as a dis-improvement within the ADC digital filter bandwidth

immediately either side of the clock frequency. (At the exact clock frequency, the interferer would be aliased to DC and not be seen by the FFT)

.

Modified sigma-delta ADC tested when directly powered from a switching regulator.

The modified sigma-delta ADC was measured for power supply rejection when powered directly from a buck switching regulator digitizing a near full-scale 1 kHz input signal. The power supply ripple frequency could not be swept as the switching regulator was designed to operate at a single external clock frequency of 2 MHz, as shown in Figure 4-20.

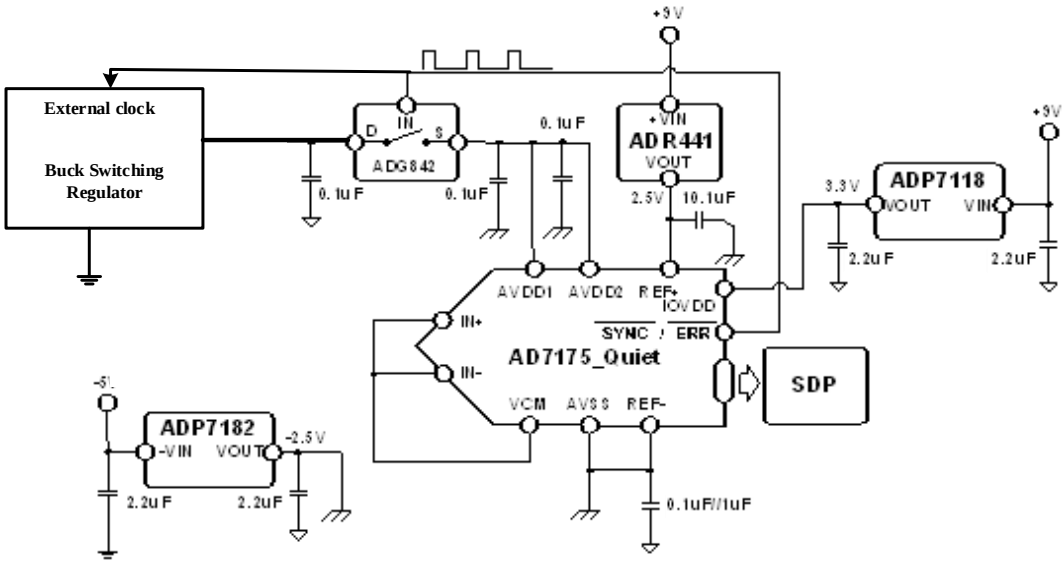
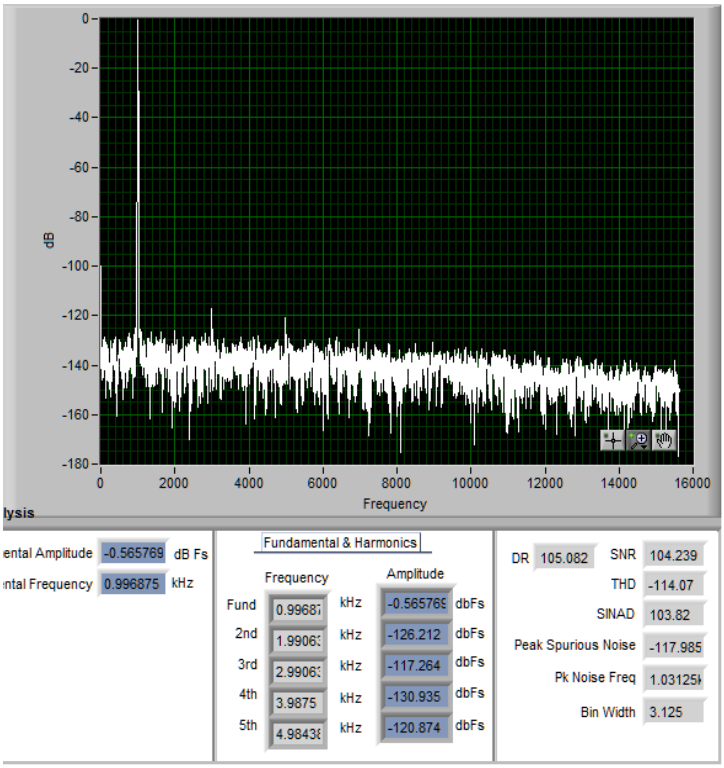


Figure 4-20 Sigma-delta ADC AC PSRR measured with a synchronized switching regulator

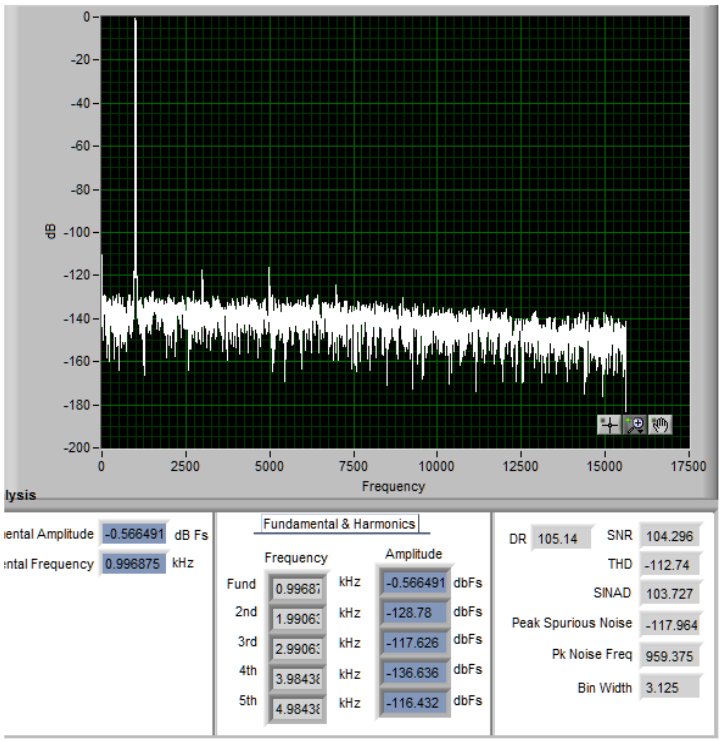
It was anticipated that running the switching regulator clock from the supply-sampling signal would cause the ripple fundamental frequency to equal the sample rate, alias

back to DC and be unseen by an FFT. It was then asked whether having the supply-sampling switch operating or just permanently on would change the result, through the introduction of other unintended switching artefacts. Such an approach may be used to explore what other frequencies might be introduced by the supply-sampling idea if the fundamental ripple is aliased to DC.



Sigma delta ADC powered from external switching regulator with clock synched to be quiet signal and be-quiet switch operating

Figure 4-21 A sigma-delta ADC directly powered from a clock-synchronized switching regulator, through an operating supply-sampling switch



Sigma delta ADC powered from an external switching regulator. The regulator clock was driven from the be-quiet signal from the ADC. The be-quiet switch was forced permanently on.

Figure 4-22 A sigma-delta ADC directly powered from a clock-synchronized switching regulator through a permanently on supply-sampling switch.

4.4.2 **Discussion of results from the modified sigma-delta ADC.**

In Figure 4-19 the supply-sampling switch is giving 1 effective bit (6dB) of improvement in those otherwise sensitive zones where the power supply interferer gets through to the sigma-delta ADC output. Only 6dB improvement is achieved in this zone of sensitivity around Fconversion because the alias at Fconversion-Fin now falls near DC where the digital filter has low rejection and it is the alias that is getting through. In the SAR ADC that alias occurred in the zone of maximum power supply rejection.

Because the sigma-delta ADC has narrow regions of power supply ripple susceptibility, the overall advantage gained is less than for SAR ADCs. Sigma-delta ADCs don't exhibit the gradually declining AC PSRR with frequency profile that this technique relies upon.

When a test was carried out with a synchronized buck switching regulator, the measured results obtained with the supply-sampling switch operating in Figure 4-21 and permanently on in Figure 4-22 a comparison of the key metrics is shown in Table 3.

	Sigma delta ADC powered from synchronized switching regulator	
	Be-quiet switch	
	Operating	**Permanently on**
SNR (dB)	104	104
THD (dB)	-114	-114
Fundamental (dBFs)	-0.56	-0.56
2nd harmonic (dBFs)	-126	-128
3rd harmonic (dBFs)	-117	-117
4th harmonic (dBFs)	-130	-136
5th harmonic (dBFs)	-120	-116

Table 3 Comparison of results obtained from a regulator clock synchronized Sigma-delta ADC with and without a supply-sampling switch.

The only significant difference seen is on the fourth and fifth harmonic levels. It is not related to the mark space ratio of the switcher clock as they are the same in both cases and determined by the internal timing of the supply-sampling signal from the ADC. Because synchronizing the supply-sampling signal to the switching regulator

clock aliases the fundamental ripple to DC, any other ripple attenuation effect is overridden.

Use of the supply-sampling signal, without any switch, to drive the clock of the external switching regulator was seen as effective to alias the ripple frequency down to DC. But there was no further significant advantage or disadvantage to using the supply sampling technique with an external synchronized switching regulator because the ripple is effectively all aliased to DC. SNR was unchanged by the presence and operation of the sampling switch, once the fundamental ripple was aliased to DC. There were no observable extra frequencies introduced by the action of the supply sampling switch.

The same benefit could have been achieved by simply driving the switching regulator clock from the conversion clock of the sigma-delta ADC.

4.5 Chapter summary

This chapter proposed a hypothesis that a totally new approach to improve power supply ripple attenuation for a mixed-signal load was possible. The power supply to the load is split into two, one for insensitive and one for sensitive circuitry. The insensitive power supply is then used to power a track and hold on the sensitive power supply, thereby attenuating power supply ripple to the sensitive circuitry. The basis for this attenuation was the use of the sinc function attenuation that occurs where a zero-order hold is used after sampling. Two different ADC architecture examples were tested, a SAR and a sigma-delta. Despite the limitation that multiple, un-

modelled, parasitic coupling paths can alter the measured results achieved in testing AC PSRR it was demonstrated that in both cases an improvement in AC PSRR was measured for the ADCs modified to incorporate the supply-sampling switch. It has been shown that the same ADC, in the same test board, tested with the supply-sampling switch shorted or operated normally was alone sufficient to cause the improvement seen in AC PSRR to be removed or added. The possibility that the improvement was even in part due to an RC filtering effect caused by the supply-sampling switch in conjunction with the supply-sampling capacitor was ruled out because the corner frequency for such a filter was above the range of test frequencies used.

The conclusion is that use of a track and hold on the power supply to an ADC prone to power supply ripple interference that has some insensitive times in its conversion period, can be shown to give a measureable improvement in AC PSRR.

Chapter 5 A ripple filter based on automatically-tuned parallel resonance using a barium strontium titanate variable capacitor.

Chapter 2 discussed the spectral content present at the output of buck switching regulators operated in CCM PWM mode, as are typically used in mixed-signal power rails. The common techniques used to filter this spectral content were introduced and compared. Chapter 3 presented the susceptibility of mixed-signal loads to such spectral content. It was seen that a system which could selectively filter the fundamental and low order harmonics of the regulator output ripple would be optimum. Chapter 4 presented a novel architecture to attenuate power supply ripple to sensitive islands of an ADC. The aim of this chapter is to present a novel scheme to notch out the ripple fundamental. Simulations and physical results involving both new die and new packages are presented. Problems encountered and solutions to those problems are included. A US patent (US 8885376) has been granted on the basic scheme and two further US patents are pending on the solutions invented to overcome implementation problems encountered.

The key metric is attenuation of the ripple fundamental for a given area penalty. Based on the summary of the state of the art in Table 1, the goal is to exceed the 60 dB available from a linear regulator with a penalty of one volt dropped, or the 40 dB from each stage of a low pass filter with a penalty of having to place the corner frequency one decade below the fundamental switching frequency leading to large inductors with higher series DC resistance (DCR).

The filter requirements for a buck regulator powering a precision analog load add considerable size, weight and power to the total design. Knowledge of the ac power supply rejection profile of such loads and cognisant that the ac content at the regulator output is dominated by energy at the switching ripple fundamental [7], [8] , [38] lead to a novel filter solution whereby a compelling saving in filter volume and power is achieved.

There are many well-known filtering techniques available, all of which are functional, but use of parallel resonance has not been commonly used in power supply filters. That is because a necessity exists to automatically tune the resonant frequency to align with the switching regulator ripple fundamental frequency [39]. With the recent availability of barium strontium titanate varactors that have values in the nano Farad range, which can be used to automatically tune to typical switching regulator frequencies, parallel resonance now represents a compelling option when the combined measures of size, weight and power loss are simultaneously applied.

5.1 Filtering Techniques.

Active power-supply ripple filtering is usually achieved using a linear regulator. The regulator derives its power from the supply to be filtered. Other active filter circuits are possible but deriving a low-noise power rail for the high-current operational amplifiers in the filter introduces a relocated, but unsolved, power-filtering problem. Modern, high-end linear regulators such as [40] offer attenuation of greater than 60 dB at typical switching frequencies (c. 1MHz) with a package volume of $9mm^3$. However,

low-noise, linear regulators require at least 0.75V voltage drop to achieve this attenuation. Size and weight are favourable with a linear regulator, but power efficiency is not.

Multi-phase regulators offer reduced ripple but at the expense of added circuit complexity [12].

Passive, low-pass, LC filters are commonly used and can be of high order. Placing the corner frequency at a sufficiently low frequency such that the desired attenuation is achieved at the power-supply ripple fundamental-frequency requires the LC product to increase in an inverse squared law relationship to the frequency, ($F = 1/2\pi\sqrt{(LC)}$).

Notwithstanding increments in standard package sizes, the area and weight of a given LC filter product are proportional to the LC product. In addition, larger inductance values lead to a higher series resistance with a consequent voltage drop incurred. Trading down inductor size at the expense of the capacitor size is limited by the required damping factor of the filter and other considerations [41].

Furthermore, higher-order low-pass filters can be less attractive options in some applications because if the low pass filter cut-off frequency decreasing below the control loop frequency of the buck regulator and the increasing phase delay with filter order causes stability problems [42].

To overcome the limitation that passive, low pass filters require large inductors, much work has been published on the use of coupled-inductor filters [43], [44], [45], [46], [47], [48], [49]. In concept, the mutual inductance of two inductors sharing one core can give rise to physically smaller inductors than two discrete inductors for the same total inductance. [43], [45]. However, coupled-inductor filters are highly sensitive to the coupling co-efficient [47], [48]. Where coupled inductor filters use series

resonance to create a low impedance shunt path to ground for the ripple frequency, there is a high sensitivity to series resistance in the low impedance power supply environment [47].

Several papers have been published that demonstrate tuning techniques to counteract the effects of coupling tolerance issues [44], [45]. A measured 20 dB improvement is reported from the use of a tuned, coupled-inductor filter compared to the same passive component values used as a low pass arrangement, [45]

Feedforward ripple cancellation has been reported by using coupled inductor techniques [16] [49] or by added feedforward amplifiers within a linear regulator [17].

The general concept of automatic tuning of filters using variable reactance is familiar [39] [50] [51] [52] but use of varactor tuners has been limited to RF and microwave frequencies [50], [51] because varactors used to date have mainly been varactor diodes or small barium strontium titanate capacitors, whose value is generally limited to the low pF range.

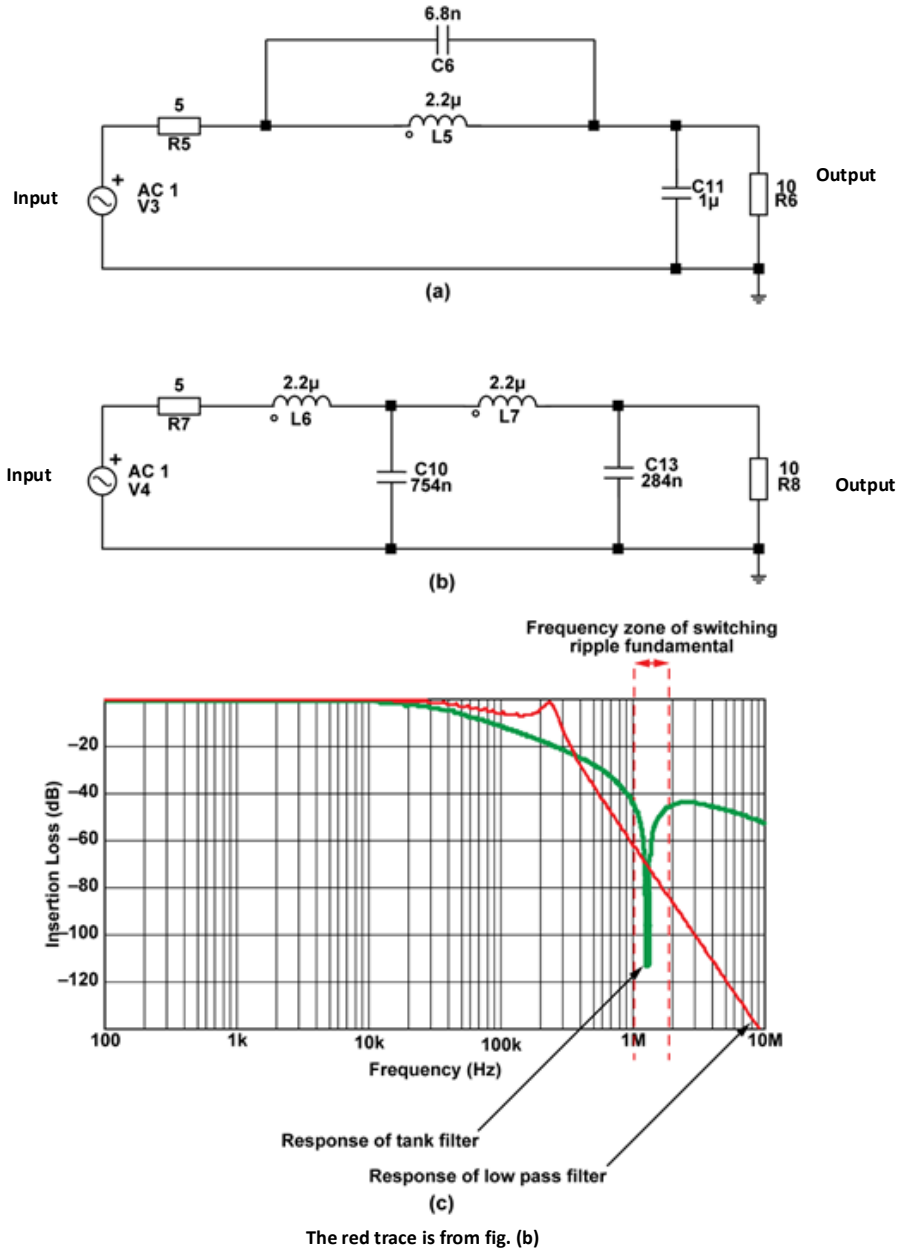


Figure 5-1 A comparison of the attenuation achieved at the switching regulator ripple fundamental (c) using parallel resonance (a)and a low pass filter (b), given a fixed 2.2 µH inductor value.

Figure 5-1 shows a Simplis [9] simulation of a fourth order low pass Fig.1(b) and a parallel resonant filter Fig 1(a), both with the a constant 2.2µH inductor value used.

The low pass implementation requires two such inductors. Yet the parallel circuit still offers 40 dB more attenuation to switching ripple as seen in Fig 1(c), if it occurs at the parallel resonant frequency.

This work uses a newly-produced barium strontium titanate capacitor with a nominal value of 18nF. Used with a novel auto-tuning technique to maintain alignment between the resonant frequency and the switching regulator ripple fundamental, parallel resonance as a power supply filter is now feasible on a manufacturable scale. Parallel resonance offers a high impedance series block to the ripple frequency and is therefore far less susceptible to degradation from parasitic series resistance than [47] demonstrated series resonance to be. The resultant power supply filter is shown to sufficiently filter a typical buck regulator output to the extent that it is adequate to directly power a precision 16-bit ADCs that have typical sensitivity to power supply borne noise, with no artefacts seen in the ADC output spectra.

The paper in reference [39] demonstrated use of tuned parallel resonance as a power supply filter but adjusted the regulator clock to tune the system. This thesis differs in that it uses varactor tuning unlike a tuned regulator clock. Tuning the regulator clock may give rise to uncertain frequency spectra. Tuned inductors are not yet available as surface mount components with sufficient Q factor at the values involved [53]

Having a varactor value of 18nF used in a resonant notch circuit results in inductor values below 10μH for typical regulator switching frequencies, which is the present day dividing line between surface-mount and through-hole inductors [54] [55]. Thus the entire regulator and filter can now be surface mounted and encapsulated in one surface mount package.

5.2 Use of parallel resonance as a power supply ripple filter.

At resonance, a parallel LC filter, exhibits some useful properties as follows:

1. It exhibits theoretically infinite impedance at its resonant frequency. No current at the resonant frequency gets through to the load when the inductive and capacitive currents are exactly equal and opposite.
2. The LC product is placed at the target frequency, not one or more decades below it, as in the case of a low pass arrangement.
3. Immediately below resonance the residual current still flowing is inductive. Immediately above resonance, it changes to capacitive. This 180^0 phase shift over a narrow frequency range is detectable with a phase detector circuit thereby allowing resonance to be located by a tuning circuit.

However, it is uncommon to find tank filters used in power supplies because of the difficulty in centering resonance on the undesired frequency component [39] and lack of available analog component manufacturer's characterization data showing that the entire spectrum does not need to be filtered for mixed-signal loads, rather than just certain discrete frequencies.

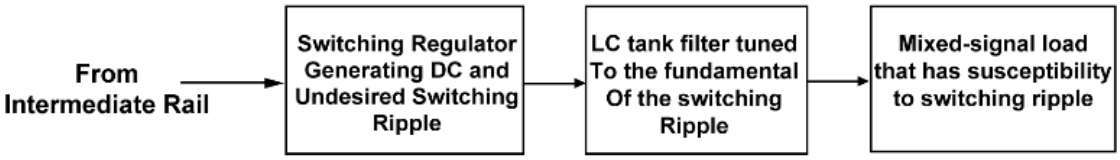


Figure 5-2 Concept of using LC resonance to filter power supply ripple between a buck regulator and a precision-analog load.

Figure 5-2 shows a concept block diagram of a single-stage parallel resonant filter used to filter power supply ripple from a mixed-signal load. In reality, the tank circuit used

as a ripple filter will not be operating independently. It will connect directly to the external load which will consist of a decoupling capacitor and a resistive element.

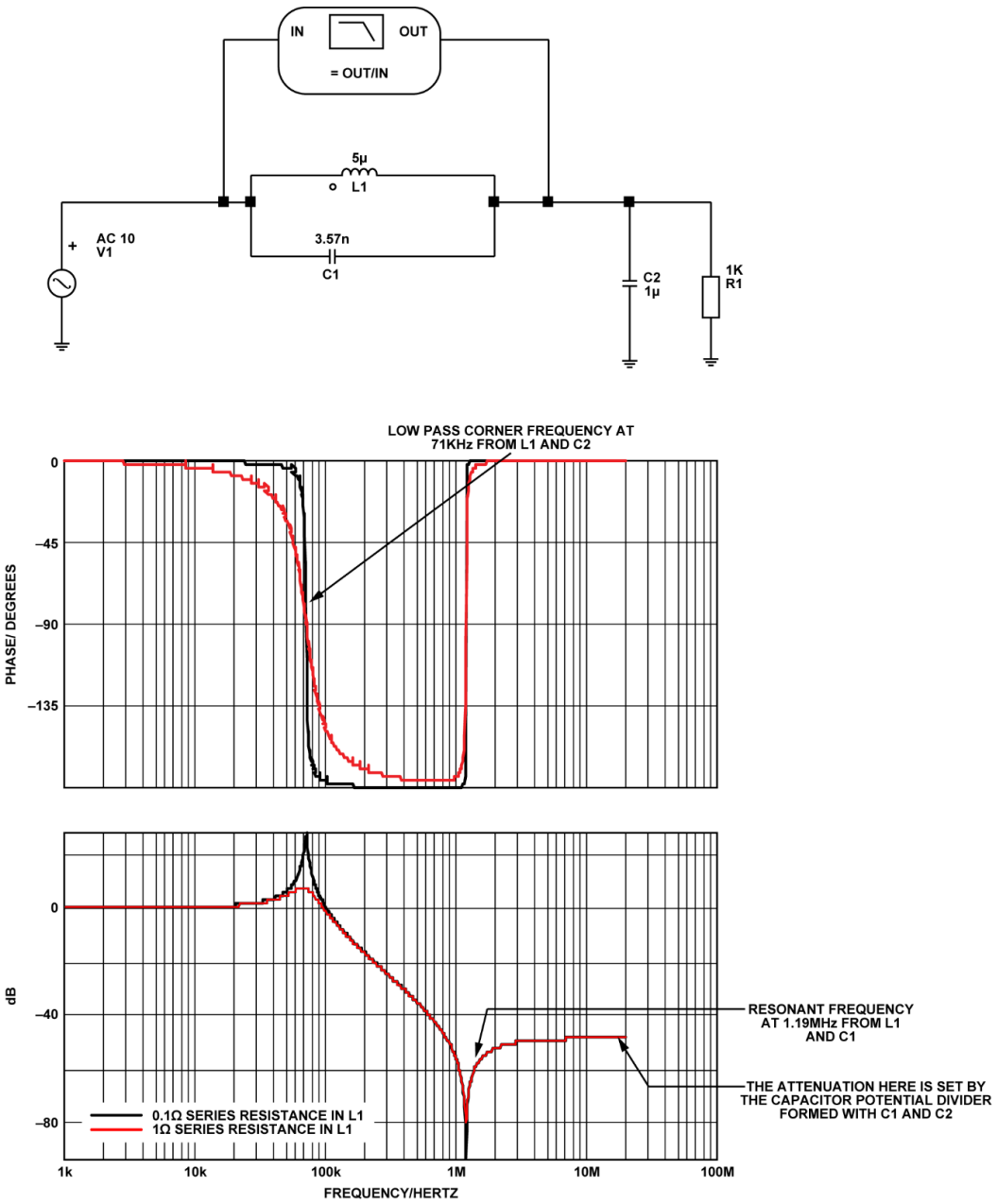


Figure 5-3 Load decoupling capacitor low pass effect on parallel resonance filter.

Figure 5-3 shows a Simplis simulation of a tank arrangement driving a 1kΩ load with a 1 µF decoupling capacitor. There are several points to note from this simulation.

1. The tank inductor, L1, forms two “different” filter elements that both aid filtering. Parallel resonance is created at the switching frequency, 1.19 MHz

in this example with C1. L1 and C2 form a low-pass filter below parallel resonance, with a corner frequency set at 71 kHz in this case. A capacitor potential divider is formed with the external decoupling capacitor, C2, which is the dominant circuit effect above parallel resonance and serves to attenuate the harmonics and other power-supply noise by a ratio of C2/C1. This ratio can be set to allow for the desired attenuation required by the load for frequencies above the ripple fundamental.

2. A 180^0 phase shift occurs at the L1 and C2 low-pass corner frequency. All frequencies above that corner frequency and below the parallel resonance frequency will be inverted by 180^0.
3. Although this filter is placed outside the feedback point from a loop stability perspective and regulator designers include a compensation network designed to degrade the regulator loop gain to below unity at least 60^0 before the specified load reactance can cause a 180^0 inversion [56], it is noted that in the case of parasitic feedback to the feedback node, the phase change introduced by this circuit is a full 360^0 for frequencies above resonance.
4. Two cases are plotted for L1 having a series resistance of 0.1 Ω and 1 Ω . For L1 having 0.1 Ω, a simulated attenuation of greater than 100dB is seen. For the case of 1 Ω, a simulated 80 dB attenuation is achieved

5.2.1 **Automatic tuning**

Even with effective inter-inductor shielding and an otherwise perfectly centred resonant frequency, component tolerances in manufacturing may be as much as +/- 20% [57], [58] of nominal value separately, for both the inductor and capacitor. A subsequent temperature and operating current deration can be in the order of +/- 25% [57], [58]. Applying these tolerances to the resonant point, ($f = 1/2\pi\sqrt{(LC)}$), gives a worst case misalignment of component tolerance multiplied by environmental tolerance, i.e. 60% in this case. This precludes use of tank circuits as ripple filters unless a method can be found to auto-tune the resonant point to the ripple frequency. [39] proposes a technique whereby this is achieved by controlling the clock to the switching regulator such that the switching frequency is aligned with the resonant notch or alternatively using a tuned inductor. This thesis proposes a different technique whereby the resonant notch is re-tuned to the switching regulator clock through the tank capacitor. This avoids the unwanted situation where the clock frequency is variable causing an uncertain interference spectrum.

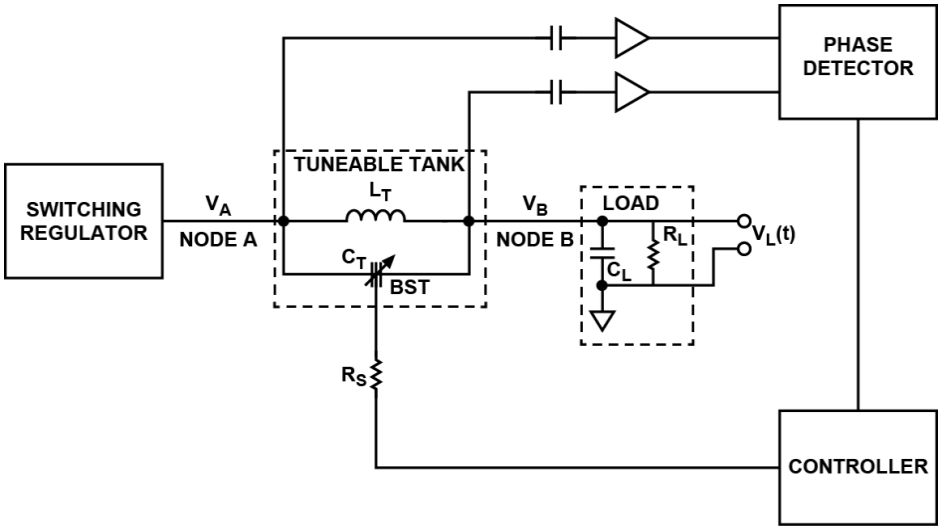


Figure 5-4 Phase lock tuning

A method is proposed whereby the phase difference between input and output voltage is measured and compared between the input and output of the tank circuit. Figure 5-4 shows a concept where the tank input at A, $Va = A_1 Sin(wt + \emptyset_1)$ and the tank output at B, $Vb = A_2 Sin(wt + \emptyset_2)$ are multiplied together and then low pass filtered. This can be shown to result in

$$VaVb = \frac{A_1 A_2}{2}[Cos(\emptyset_1 - \emptyset_2)] \qquad \text{Equation 6}$$

Equation 6 suggests that a DC term results that is proportional to the cosine of the phase shift though the tank. This phase detection method can be used to detect resonance and tune the circuit to maintain resonance centering. The action of the external decoupling capacitor is to introduce a 90^0 phase shift. This in turn causes resonance to centre on a 90^0 phase shift, instead of 0^0 as would have happened without the external capacitor. The cosine term in Equation 6 is a cosine of 90^0 allowing a DC

polarity change to be detected either side of resonance. Reference [39] multiples a voltage by a current, requiring a current sensing transformer. The method proposed here multiples two voltages. The monotonic nature of tuning about a cosine which is positive above resonance and negative below resonance simplifies the tuning circuitry.

In practice, node A will not have a single frequency but rather a fundamental, harmonics and interferers. To examine what happens in the case of two frequencies at node A, with amplitudes A1 and A3 and frequencies respectively wt and x*wt

$$Va = A_1 Sin(wt + \emptyset_1) + A_3 Sin(x\,wt + \emptyset_3)$$

$$Vb = A_2 Sin(wt + \emptyset_2) + A_4 Sin(x\,wt + \emptyset_4)$$

$$\begin{aligned} V_a V_b = {} & A_1 A_2 Sin(wt + \emptyset_1) Sin(wt + \emptyset_2) \\ & + A_1 A_4 Sin(wt + \emptyset_1) Sin(x\,wt + \emptyset_4) \\ & + A_3 A_2 Sin(wt + \emptyset_2) Sin(x\,wt + \emptyset_3) \\ & + A_3 A_4 Sin(x\,wt + \emptyset_3) Sin(x\,wt + \emptyset_4) \end{aligned}$$

Which after the low pass filter is:

$$Va\,Vb = \frac{A_1 A_2}{2} Cos(\emptyset_1 - \emptyset_2) + \frac{A_3 A_4}{2} Cos(\emptyset_3 - \emptyset_4) \qquad \text{Equation 7}$$

The loop action is to make the product Va*Vb in Equation 7 equal zero thereby attempting to make the cosine of the phase delay seen by both components equal and opposite (assuming equal A1.A2 and A3.A4 magnitude terms). This will cause the

loop to centre resonance at a point where the two phase delays are equally spaced about 90^0. If the second or subsequent harmonics become larger as the application is modified, the auto tune circuit will tune to optimally attenuate the mean.

An alternative method of 'perturb and observe' tuning was considered. This tuning technique would involve making a change to the tuning element and observing the magnitude of the AC content at the output. If the AC content increases, the tuning element is driven in the opposite direction and vice versa. The challenge with this technique is that the solutions have the potential to completely miss the resonant zone in a high Q (meaning narrow 3dB bandwidth) system and jump directly between plateaus.

5.2.2 **Barium Strontium Titanate as the tuning element**

A tuning element was required that fulfilled the following criteria:

1. A Q factor of at least 20 to preserve the steep attenuation curve associated with resonance.
2. A control voltage under 10 V. This tuning circuit would to have to be powered from a supply derived in parallel with the supply that it is intended to filter. That utility supply should be low-current, low-voltage, and small such that it would not defeat the purpose of the circuit to start with.
3. It should be possible to fabricate it on chip. The ultimate goal is to reduce space in the filter system suggested.

4. In the case of capacitance, values at least in the low nF range should be available so that the tank inductance for typical switching regulator frequencies would be achievable as a surface mount component without excessive size or series resistance.
5. The breakdown voltage should exceed that seen across the tank.

Variable inductors were considered but any planar variants that could be integrated on chip that had inductances in the μH range had Q factors of less than ten [53] because the available space is limited and reduced metal thickness causes higher series resistance. Further, the tank inductor carries the full DC current that the regulator is intended to supply so heating and voltage drop would preclude the use of on-chip inductors.

Barium Strontium Titanate (BST) is known as a capacitor dielectric in the RF industry [59], [60], [61]

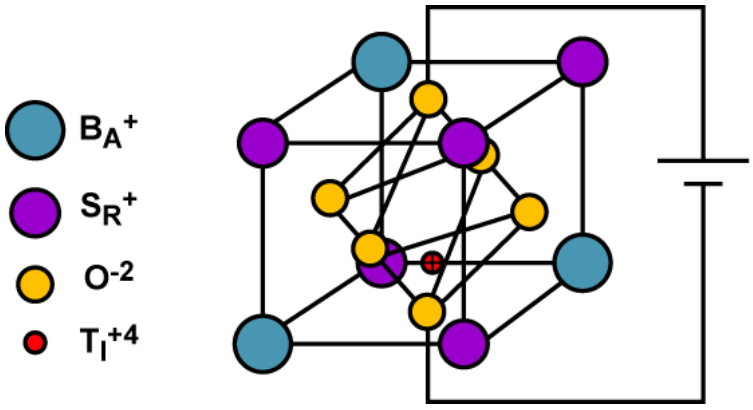


Figure 5-5 Barium strontium titanate molecular structure

The molecular structure of BST is shown in Figure 5-5. It has a mobile positive titanium atom that displaces easily with applied field causing paraelectric behaviour, i.e. polarization varies with applied voltage causing the relative permittivity to vary and consequently the capacitance as shown in Figure 5-6.

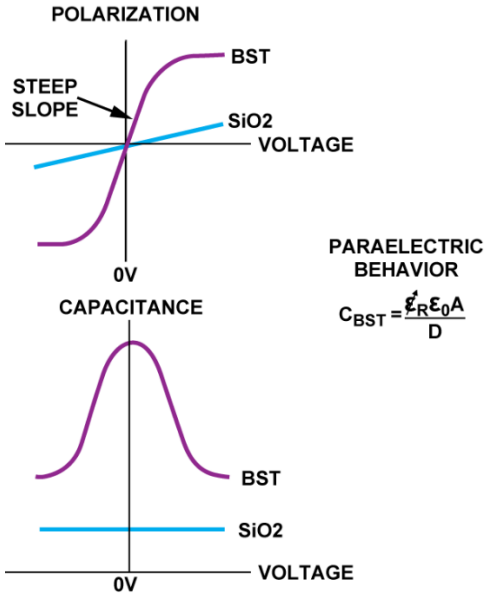


Figure 5-6 Paraelectric behaviour of BST compared to non paraelectric SiO_2

BST offers some useful properties in this case.

1. Breakdown voltage of 18 V
2. Tune-ability (Cmax/Cmin) of 3 from 0 V to 10 V
3. Q factor of 20 at 1GHz
4. Relative permittivity of 475
5. Capacitance density of 20 fF per square micron (18 nF for this application requires 1 square mm of plate area)
6. Cmax change of 22% from 0^0 to 125^0 centigrade.

With industry-wide decreases in wafer-fabrication defect-density it is now feasible to fabricate areas of barium strontium titanate dielectric with a thickness allowing tens of nanofarads of capacitance with manufacturing yields that allow costs to be in line with any other wafer that has a similar number of mask steps. A voltage variable capacitor using a 0.2μm BST dielectric thickness was fabricated. Figure 5-7 shows a cross section taken using a scanning electron microscope. Two 18 nF BST capacitors were

connected in series to allow a DC control voltage to be applied to an AC path. The capacitance versus applied voltage profile is shown in Figure 5-8. A die photograph showing a planar view of the two capacitors is shown in Figure 5-9

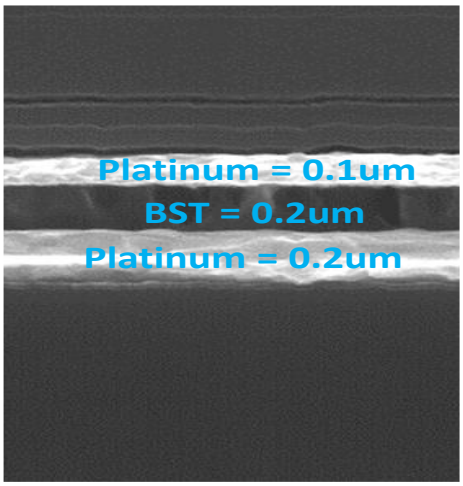


Figure 5-7 BST varactor cross sectional view

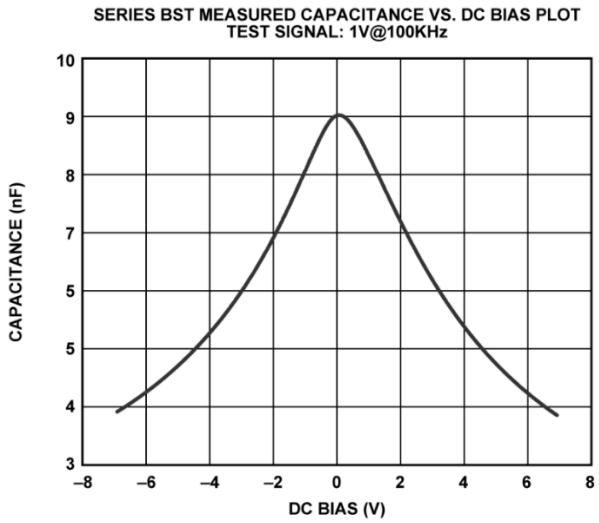


Figure 5-8 Capacitance versus applied voltage for BST tuning element

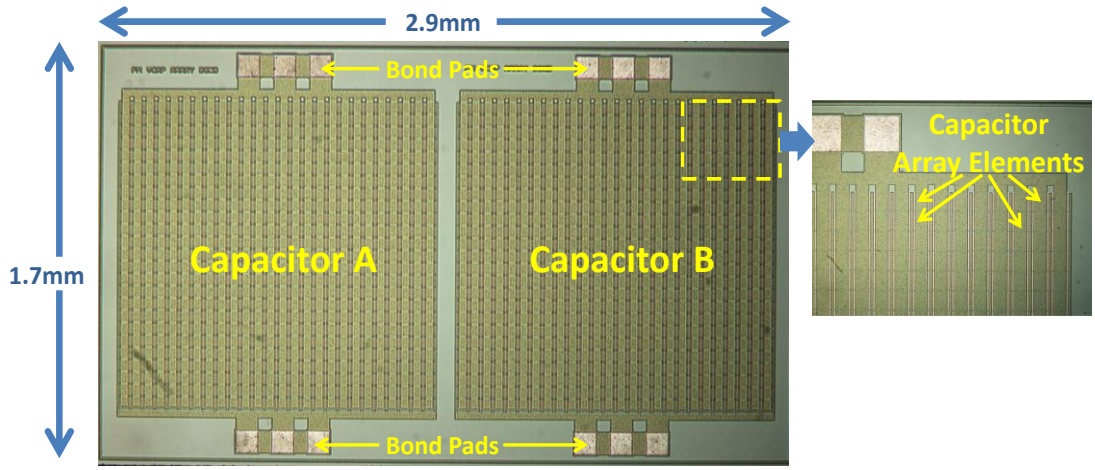


Figure 5-9 BST varactor planar view

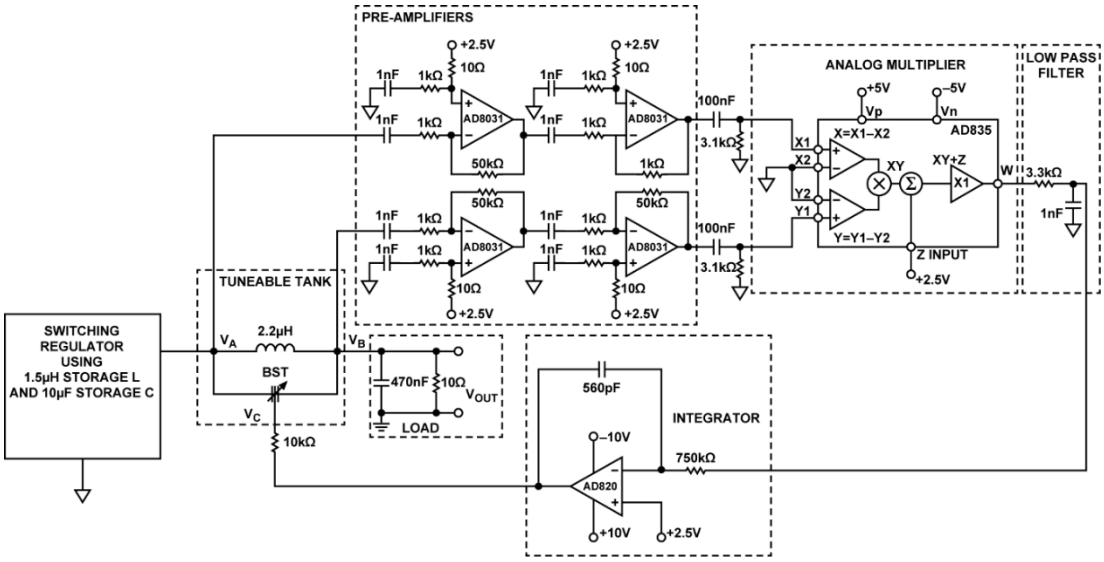


Figure 5-10 BST based automatic tune schematic

The prototype schematic used to implement the automatic tuning (auto-tune) circuit using the BST capacitor from Figure 5-9 is shown in Figure 5-10. Some pertinent points are mentioned below :

1. The pre-amplifier gain is set at 50 for Va, the input to the tank and 2500 for Vb, the output of the tank. The predicted ripple magnitude needs to be considered in setting these gains. If the gain is too high will saturate the amplifiers, if it is too low it will allow the multiplier offset (25mV) to introduce relatively too much error.
2. The active components used require several different voltages, ranging from 2.5V to 15V DC. It is envisaged that this entire circuit could be powered from a very low current charge pump in an integrated solution
3. The maximum tuning range of the filter is limited by the tolerance of both the tank inductor (20%) and the varactor. The varactor tolerance budget comprises manufacturing tolerance, ageing and temperature. But as the two varactors are manufactured together and will be at a very similar temperature, the actual spread seen on prototype runs has been just 2%. It is envisaged that a manufacturing trim could be applied to centre the initial start-up conditions.
4. Consideration must be given to the resonant point of the tank inductor and external decoupling capacitor such that it does not occur within the tuning range. A high-pass filter comprising a 1nF capacitor and 1kΩ resistor is positioned on the input of each amplifier for that purpose.
5. The auto-tune circuit is suitable for the normal range of switching regulator frequencies (c500 kHz to 2 MHz) but would not suit lower

frequency systems where the ripple frequency coincided with the corner frequency of the low pass element.

6. While use of parallel resonance greatly reduces the detrimental effect on ripple attenuation posed by series resistance to series resonant arrangements, a parallel arrangement will prove more sensitive to the parasitic parallel resistance inherent in inductors. This parasitic value can be as low as 1 kΩ for surface mount inductors [54].

5.3 Results

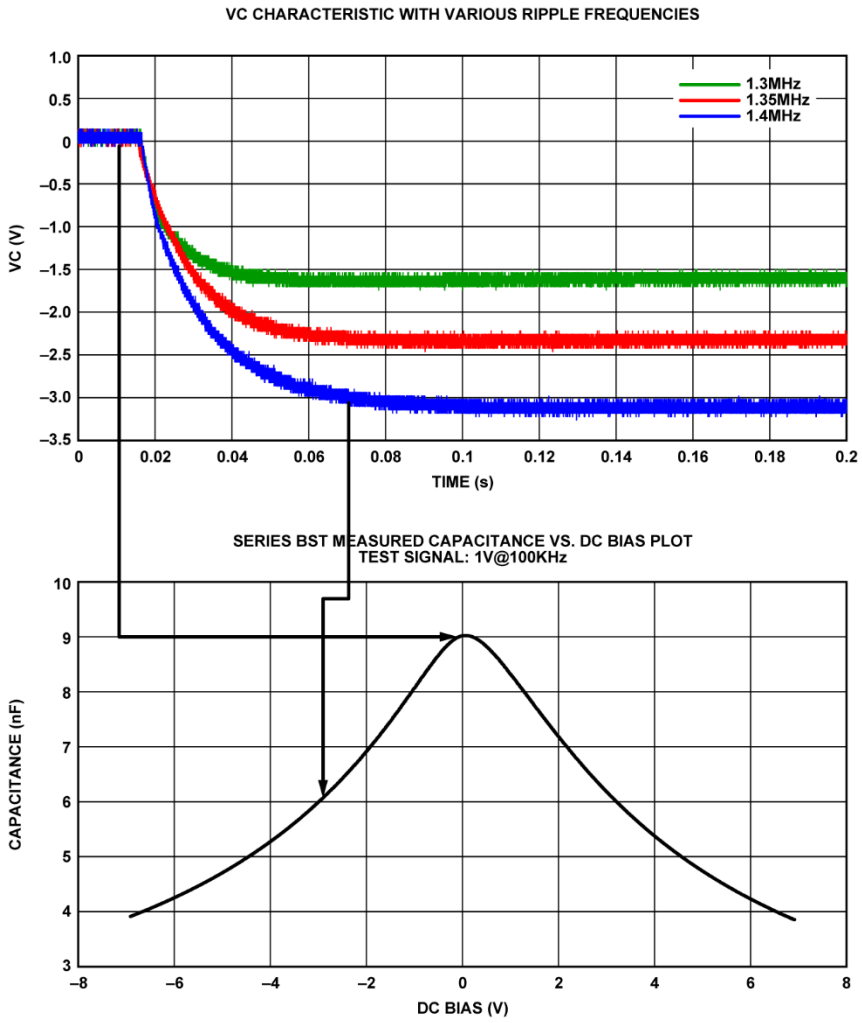


Figure 5-11 Lock-in time and voltages

The measured voltage/time profile of the integrator output voltage, Vc, applied as the tuning voltage to the BST capacitor, measured relative to Va is shown in Figure 5-11. Ideal PWM test waveforms with three different test frequencies were used: 1.3 MHz, 1.35 MHz and 1.4 MHz. When the 1.4 MHz trace is overlaid against the BST characterization data shown in Figure 5-8 and repeated in Figure 5-11, it is seen that the BST capacitor starts at 9 nF, equating to a 1.13 MHz resonant frequency with the 2.2 uH tank inductor used. After 70 mS, the system has tuned to a -3.3 V tuning voltage, suggesting a 6 nF BST capacitor value, equating to a 1.4 MHz resonant

frequency. That is exactly the switching clock frequency the regulator was set to for this experiment.

Figure 5-12 shows a time domain oscilloscope trace showing the regulator clock, the tank input and the tank output.

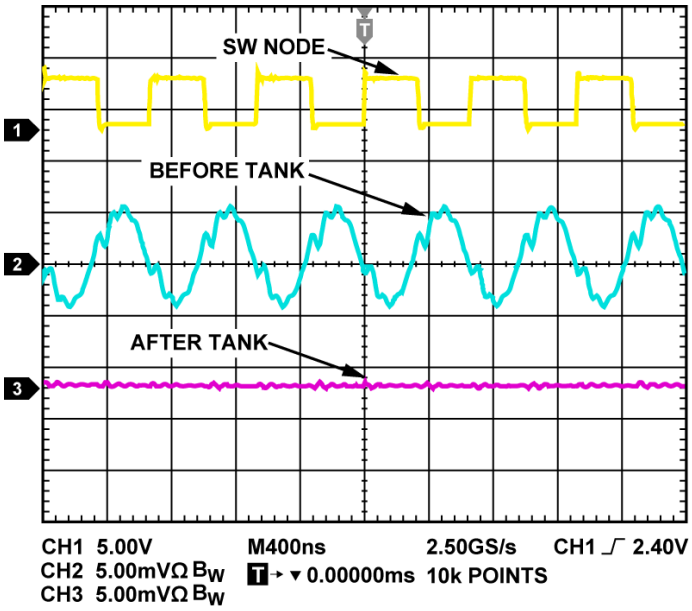


Figure 5-12 Oscilloscope plot of the switch node, the input to the tank and the filtered output

5.3.1 **Tests carried out with a buck regulator.**

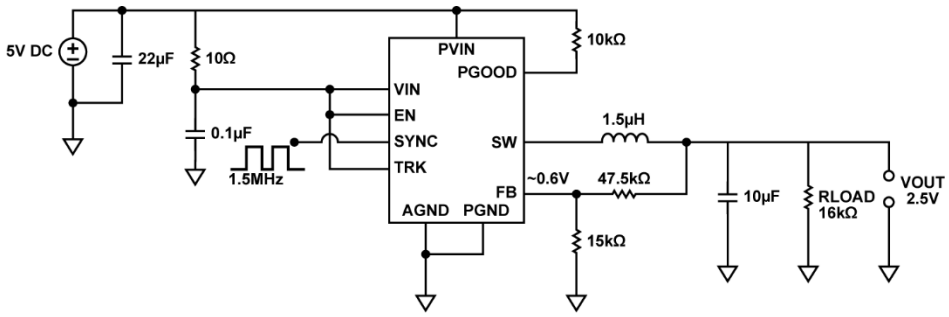
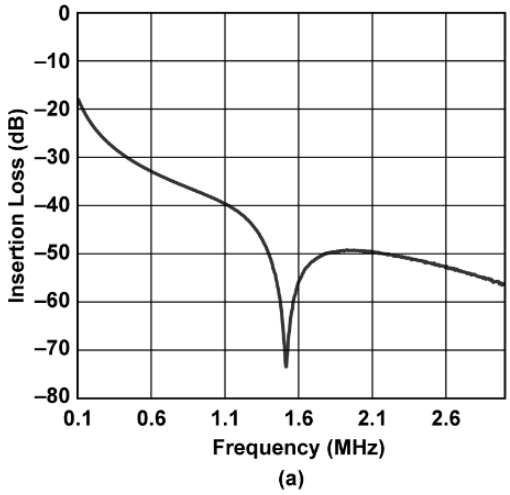
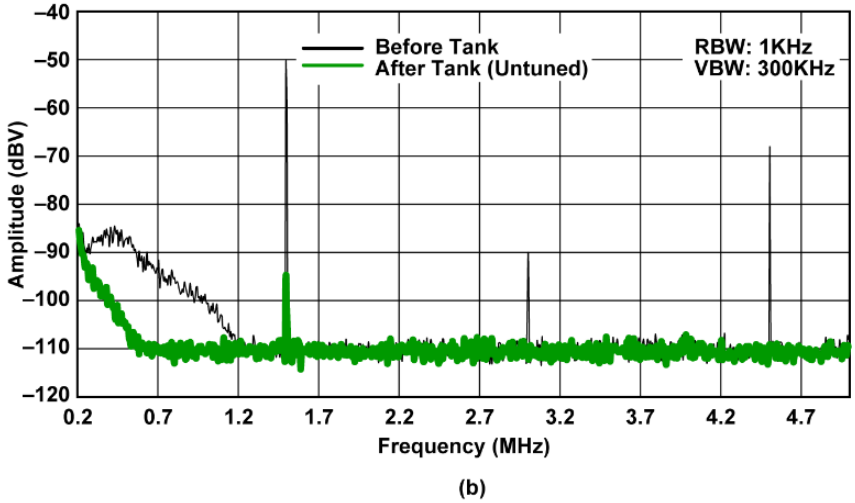


Figure 5-13 ADP2120 buck regulator schematic used to test the auto-tune tank filter





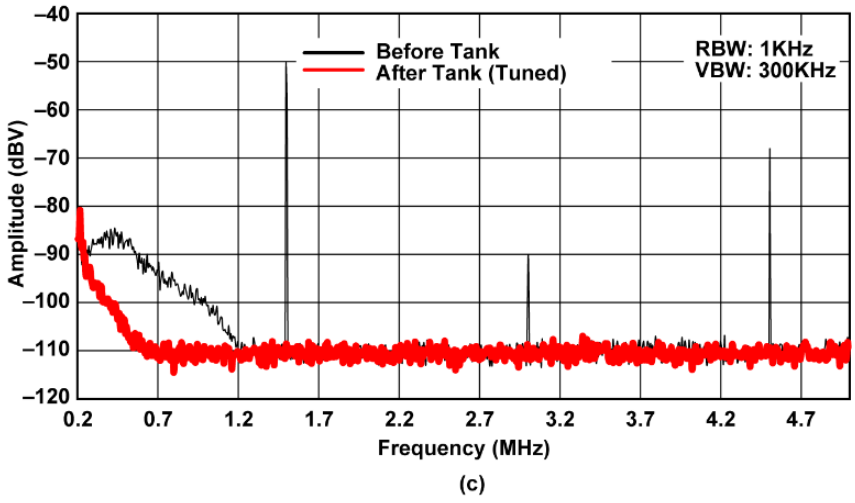


Figure 5-14 Frequency domain results (a) of tank (b) switching regulator output with un-tuned tank and (c) switching regulator output with tuned tank.

Figure 5-14 shows the frequency domain results achieved when the auto-tune filter in Figure 5-10 was used with the ADP2120 buck regulator schematic shown in Figure 5-13. The regulator clock was set to 1.5 MHz. Plots are shown for the two cases of un-tuned and tuned operation. The extent of the difference would depend on how "un-tuned" a given setup was. The purpose of these results is to demonstrate that in this particular case, tuning attenuated the ripple from -95dB to below the noise floor at -110dB.

5.3.2 **Tests carried out on a 16 bit ADC.**

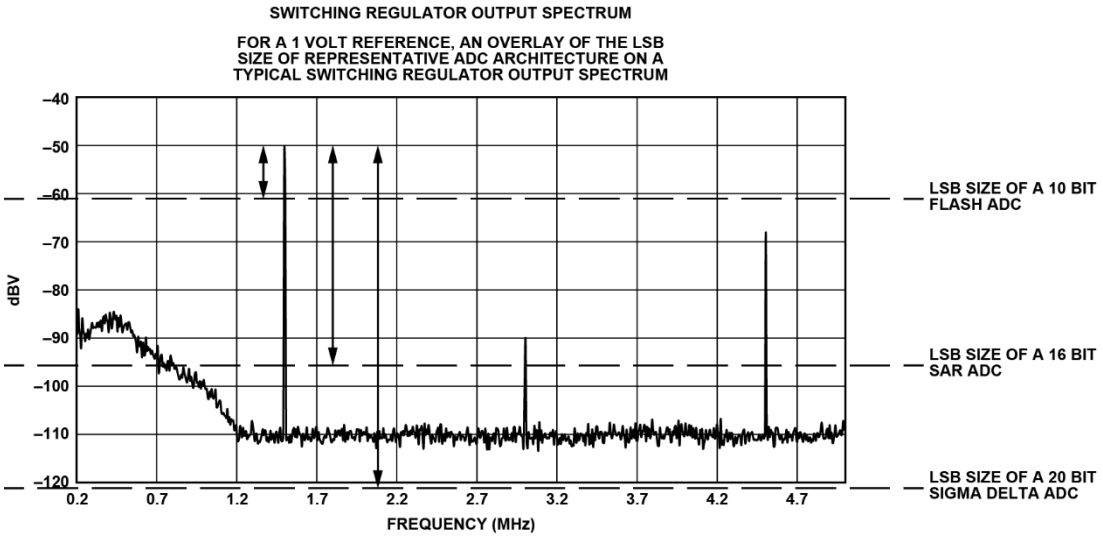


Figure 5-15 Switching regulator output spectrum with various ADC LSB sizes overlaid

Figure 5-15 (previously seen in Figure 3-2) shows the power supply output spectrum from the schematic shown in Figure 5-13 with the LSB size of three different resolution ADCs, given a 1 V reference, overlaid. It would be normal to attenuate interferers to less than 10% of an LSB size to minimize the error caused at a bit-trial threshold.

A 16-bit ADC, the AD9268, was tested both directly powered from the switching regulator and then powered via the auto-tuned tank, i.e. from node Va and then node Vb in Figure 5-10, with the spectral content as shown in Figure 5-14. The ADC sample rate was 125 MSPS. It had a 470 nF external decoupling capacitor and was digitizing a 40 MHz near-full-scale signal. Figure 5-16 shows the fast Fourier transform (FFT) of the ADC output when powered from node Va. The 500 kHz band noise and the fundamental ripple frequency seen in Figure 5-14 degrades the useable dynamic range by approximately 20dB. Figure 5-17 shows the same ADC output when powered from node Vb. The power supply artefacts are successfully attenuated to below the ADC noise floor.

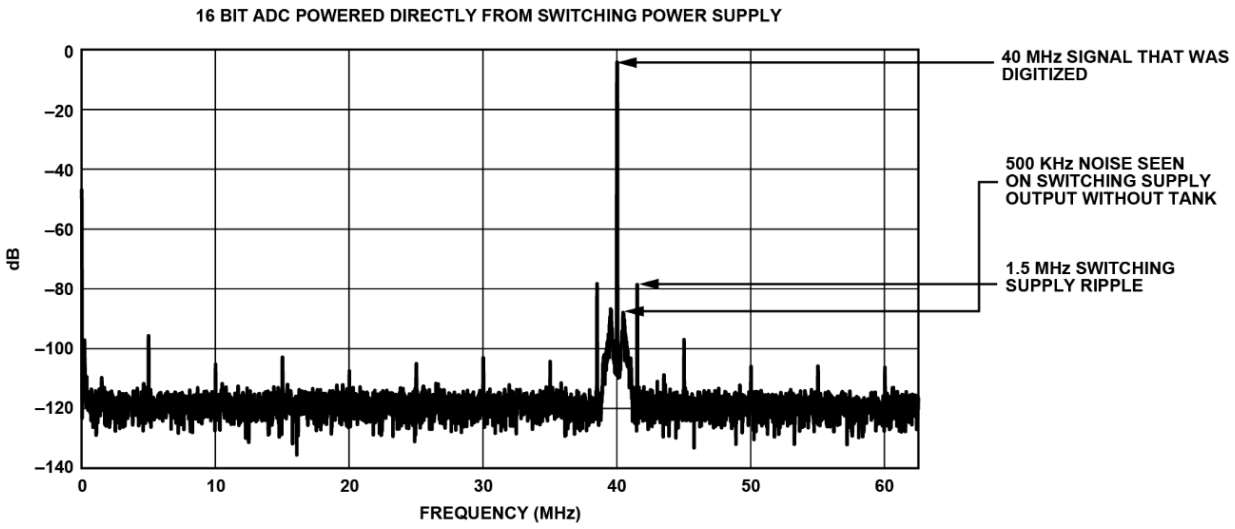


Figure 5-16 FFT of a 16 bit ADC output when powered directly from a switching regulator.

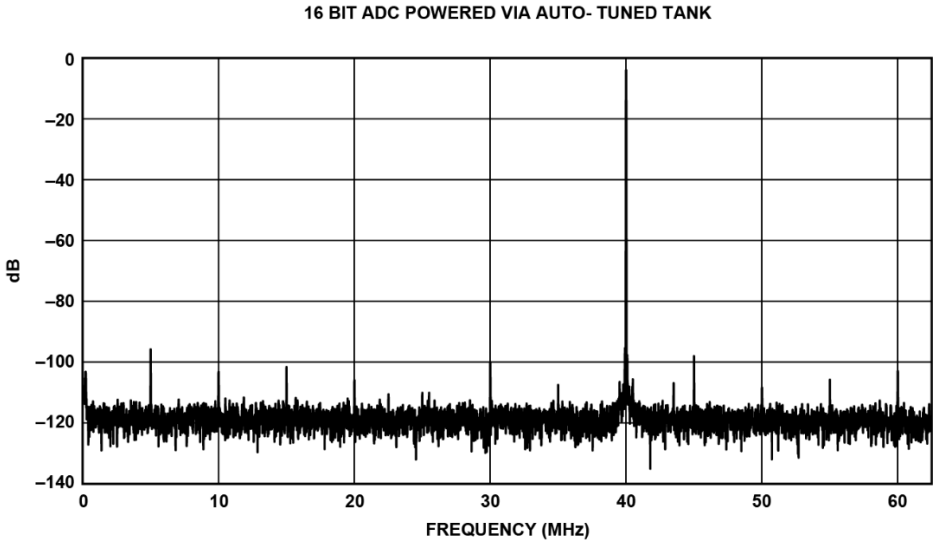


Figure 5-17 FFT of 16 bit ADC output powered via BST auto-tuned tank

5.3.3 **Single-package surface mount encapsulation.**

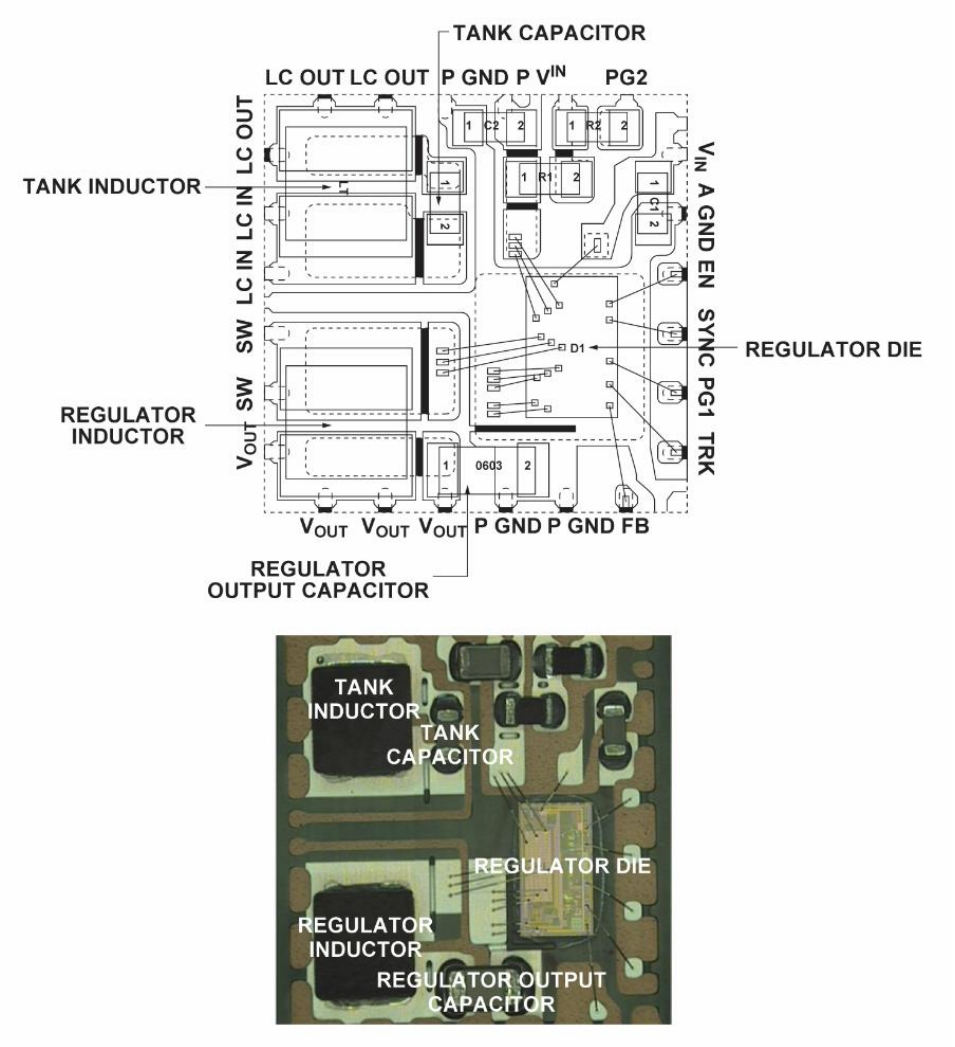


Figure 5-18. 7mm by 7mm LFSP package encapsulation of entire switching regulator and an un-tuned tank

Figure 5-18 shows a full surface-mount, single package version, without the auto-tune circuitry, which contains the entire ADP2120 buck regulator, all external components in addition to the tank inductor and a single tank capacitor. The high fraction of the available space used by the regulator-output inductor and tank inductor are visible. Successful use of the tank circuit to attenuate ripple opens the possibility to further

shrink the regulator-output inductor, as the increased ripple resulting can now be successfully attenuated.

5.3.4 **Physical volume required.**

The area required by this solution is shown in Table 4. The inductor size used for the example low-pass filter was governed by the requirement to handle at least 1 A and with a low series resistance.

FILTER TYPE	COMPONENT	MANUFACTURER / MODEL	VALUE	DCR (MAX) mΩ	DIMENSIONS (mm)				
					L	W	H	VOL (mm^3)	TOTAL VOL (mm^3)
AUTOTUNED TANK	TANK INDUCTOR BST CAPACITOR TUNING CIRCUIT OUTPUT CAPACITOR	TOKO DFE252010P IN HOUSE FAB ESTIMATED DIE AREA MURATA MLCC GRM155 (0402)	2.2µH 3 TO 9nF	115	2.5 2.9 3.0 1.0	2.0 1.7 2.0 0.5	1.0 0.1 1.0 0.5	5.0 0.5 6.0 0.3	11.7

Table 4 Volume required to implement the auto-tuned tank filter

To supply 1 A, the auto-tuned tank will drop just 100mV across the inductor DCR. The best available linear regulator [40] requires 750mV dropped and a similar volume (9mm^3 versus 11. 7mm^3) to offer similar (-60dB) ripple attenuation.

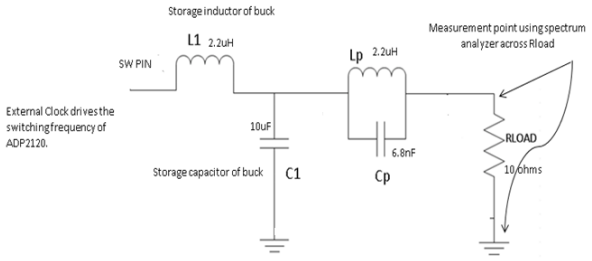
5.4 Overcoming detuning effects.

5.4.1 **Inter-inductor shield.**

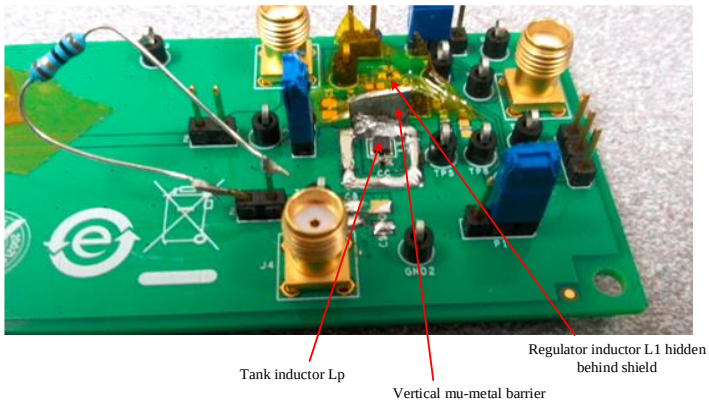
The contribution that inductor to inductor coupling has in detuning the resonance point from the desired ripple fundamental has been referred to in section 5.1 Whilst that is not the only contributor to detuning, it is addressed first.

An experiment was designed to both measure the effect of mutual inductance on the resonant point and secondly to find an effective way to shield against it. Given that the type of shielded and orthogonally placed inductors shown in Figure 5-18, are the standard approach in applications involving EMI reduction, etc., but were insufficient in this case of resonance shift, something more effective and novel was sought. The objective was to find a solution that could be implemented in the volume of a surface mount package.

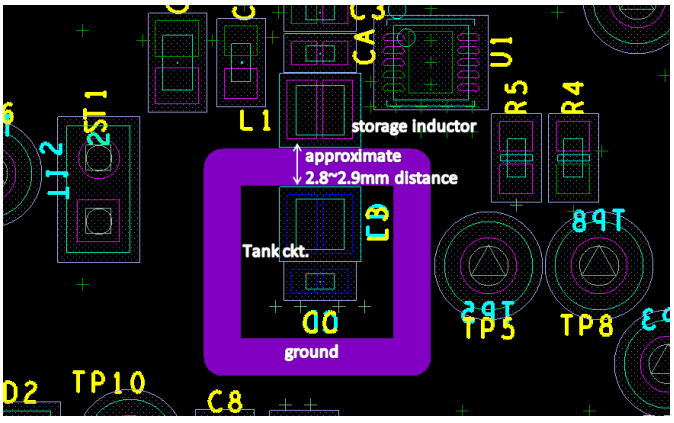
A vertical wall of a high permeability material between the two inductors was used. “Mu-metal” is a commercially available Nickel / Iron / Molybdenum alloy used for magnetic shielding. “Mu-copper” is a similar copper-based malleable product. Figure 5-19 shows the test set up used.



(a)



(b)



(c)

Figure 5-19 Test set up to evaluate mutual inductance reduction (a) schematic, (b) PCB, (c) floor plan.

The results are shown in Figure 5-20 from which conclusions can be drawn :

1. If the inductors are spaced 2.9mm apart, as would be typical in a surface amount package, mutual inductance may shift the resonant point by 17% (as can be measured from the plot labelled “w/o vertical shield”) which decreases notch depth by 10dB.
2. A high permeability vertical, grounded barrier placed between the inductors reduces the resonance shift to under 2%.with the height of the barrier having the greatest effect on the detuning shift.

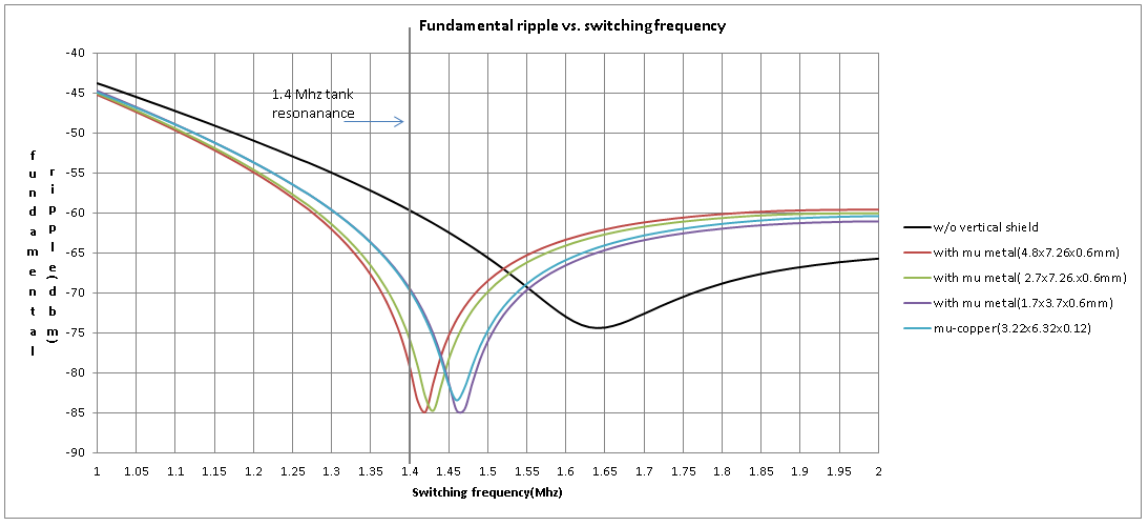


Figure 5-20 Results of mu-metal barrier

Shield(height x width x thickness)	Measured Resonance(Mhz)	Target resonance(Mhz)	% shift
w/o vertical shield	1.64	1.4	17.14285714
mu metal(4.8x7.26x0.6mm)	1.42	1.4	1.428571429
mu-metal(2.7 x 7.26x0.6mm)	1.43	1.4	2.142857143
mu -metal(1.7 x 3.7 x 0.6mm)	1.46	1.4	4.285714286
mu-copper(3.22x6.32x0.12)	1.46	1.4	4.285714286

Table 5 Tabulated results of mu metal barrier experiment

These findings led to the invention of a technique whereby a rectangular leaf is punched out in the lead frame metal and bent vertically at 90^0 during the assembly process. This technique is now the subject of a US patent application. It is shown in Figure 5-21 . An alternative is to solder a separate mu-metal barrier in place, between the two inductors, as shown in Figure 5-22.

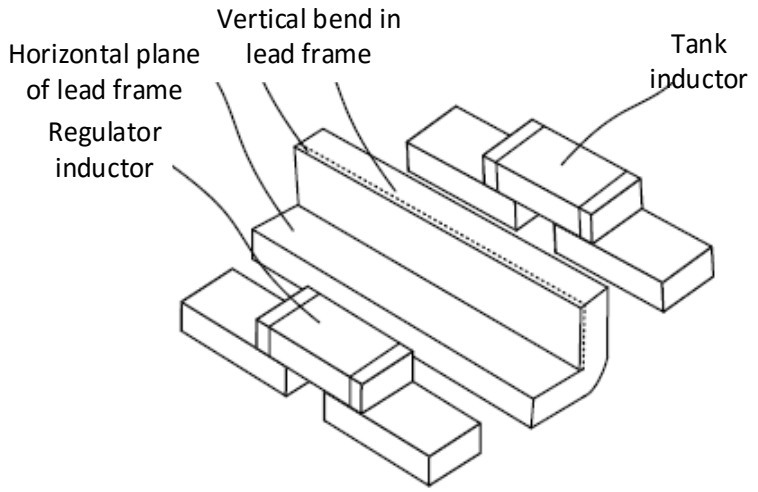


Figure 5-21 Lead frame bend to shield the resonant inductor

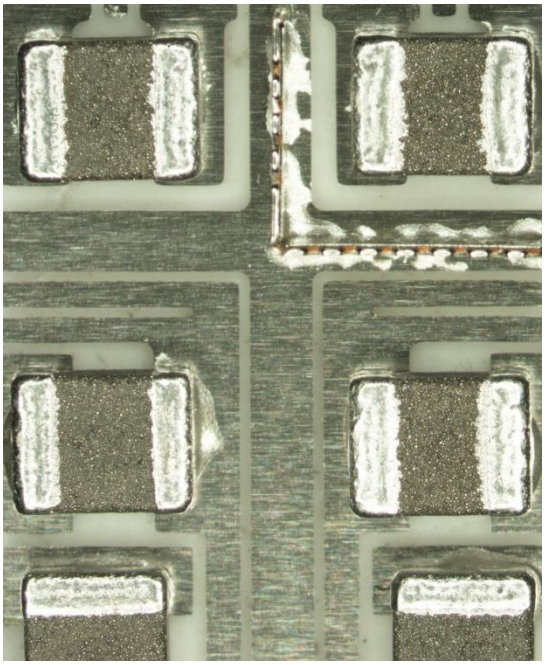


Figure 5-22 SMD package lead frame with a mu-metal barrier soldered into place prior to plastic encapsulation.

5.4.2 **Further enhancements**

In section 5.2.1 the fact that this circuit auto tunes to a mean of the frequencies at node A was discussed. A consideration here is that when the regulator duty cycle is such that the harmonics are relatively large compared to the fundamental, as shown in Figure 2-4, that causes the tuning point to be biased towards the harmonics, depending on the relative gains of Va and Vb in the circuit in Figure 5-10 An enhancement invented in this project was to incorporate a switched resistor, ("Q-reduction"), to temporarily reduce the Q of the tank circuit. This would increase the amplitude of the fundamental relative to the harmonics and cause the resonant point to bias towards the fundamental. It is part of a timed circuit where the Q-reduction scheme would be used in a calibration cycle to tune the tank and thereafter switched out. The concept of a Q-

reduction switch used with an auto-tune circuit based on a tuned capacitor system is shown in Figure 5-23. This circuit is now the subject of a US patent application.

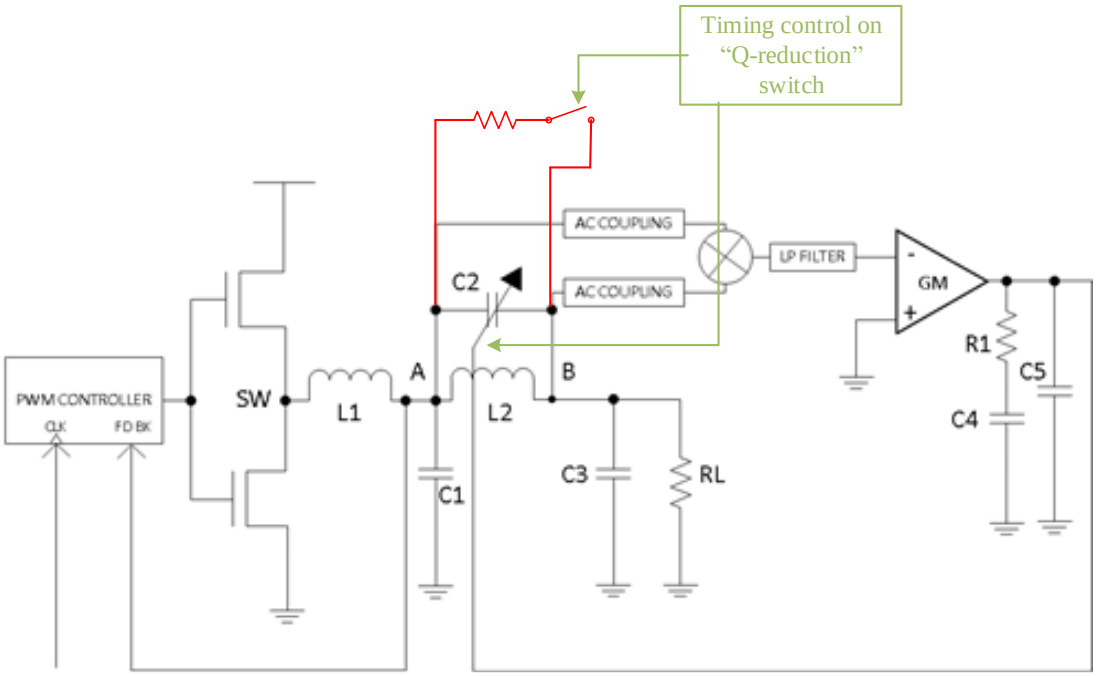


Figure 5-23 Use of a temporary "Q-reduction" switch

5.4.3 Discussion of results

Figure 5-14 demonstrates that over 60dB attenuation was achieved with the particular surface mount components used. The tuning control circuit can be integrated on chip and its supply voltages optimized. 4 mm^2 is taken as an estimate of the die area required on a low voltage process to implement the active elements of Figure 5-10 including the passives, a low-current charge pump and a linear regulator to derive the power necessary for the amplifiers and multiplier. In the case of the BST auto-tune circuit, the external decoupling capacitor is also included in the area penalty because it is a fundamental part of the circuit operation. It is shown that the auto-tune circuit

can achieve the same attenuation as an LC low-pass filter in a fraction of the volume. What that fraction is depends on the criteria governing the multi-pole low-pass alternative, such as whether the maximum DC current specification for the supply precludes the use of surface mount inductors or not. The entire circuit for the BST auto-tune circuit can be mounted on to a single lead frame. A further advantage of the BST auto-tune circuit is that the lower inductance values required lead, in turn, to smaller DC resistance (DCR) in the inductors available. Implementing the low pass filter in section 2.3.4 for a 1 A supply would cause a 0.372 V drop after the regulation loop, compared to 0.115 V for the BST auto-tune [54].

5.4.4 **Chapter summary**

This chapter presented the problems and limitations encountered in using parallel resonance as a ripple blocking technique. It was demonstrated that the advantages of using parallel resonance could be realized by auto-tuning the resonant frequency to the ripple. A novel BST varactor was produced and utilized. The solution presented is smaller and drops three times less voltage than the equivalent low pass configuration. Critically, the solution presented here is small enough to be integrated both on-chip and on-lead frame allowing the entire power supply solution to be integrated in to one surface mount device.

Further, two inventions in response to problems encountered were patented. One allows two inductors to be co-packaged where isolation exceeding that available from commercially available surface mount shielded inductors is necessary. The second invention allows the Q of the parallel circuit to be temporarily reduced while the auto-tune circuit hunts for a mean between the fundamental and harmonics.

Chapter 6 Conclusions and future work.

In this thesis it has been shown that the dominant interference from buck, switch-mode power-supply regulators intended to power mixed-signal loads is the fundamental switching frequency ripple. That ripple is primarily dependent on the storage LC product, the switching frequency and the input voltage. Selective attenuation of the ripple is sufficient filtering to allow typical, modern high-precision mixed-signal loads to be directly powered without further conditioning. A 16 bit ADC was demonstrated.

A survey of the commonly used ADC, DAC and frequency synthesiser's susceptibility to power supply ripple interference was carried out and empirical results presented. An explanation of the exact nature of sigma-delta ADC susceptibility to power supply interference was produced.

An entirely new architecture was proposed whereby the ADC circuitry was divided into those circuits which would be not sensitive to power supply ripple and those which would be, some of the time. The concept of placing a track and hold on the sensitive-node power supply and controlling it from the insensitive node power supply and timing signals was outlined. The potential to use sinc function attenuation to reduce the power supply ripple seen by the sensitive circuitry, during its sensitive time was proposed. The practical limitations to the accurate measurement of the effectiveness of this technique were outlined. Measured results from both a SAR and a sigma-delta ADC were shown which verified the hypothesis as correct.

A comparison of the commonly used power supply filtering techniques was presented. A novel method of using parallel resonance was proposed and the limitations associated with manufacturing, power, voltage and temperature shown.

An automatic tuning technique for the resonant point, based upon a newly available barium strontium titanate, voltage variable capacitor was demonstrated. An invention to overcome the high susceptibility of resonant circuits to mutual coupling between the two inductors involved was shown. A further invention to temporarily decrease the Q factor of the resonant circuit to achieve tuning biased towards the ripple fundamental frequency was outlined.

It was shown that for a typical 16-bit ADC chosen to test, the auto-tuned resonant circuit was entirely adequate as a complete power supply filter. It was further shown that the entire buck regulator and auto-tuned resonant filter could be integrated into a single surface-mount package

Future work possible from this project would include the following:

1. The unavailability of sufficiently accurate process models today precludes useful simulation to identify the exact pathways where power supply ripple couples through to the signal path. More accurate models would allow precision analog-input circuit designers to achieve better matching between branches of differential circuits and thereby improve AC PSRR.
2. Optimization of the auto-tuning circuit shown in Figure 5-10. The circuit requires its power to be derived from the circuitry being filtered. A low-current, low-noise charge-pump based circuit to derive the amplifier and integrator power supplies can be achieved.
3. Refinements can be made to the technique of applying a track and hold to the sensitive circuitry on an ADC. A non-zero order hold could give increased attenuation. An increased on-resistance would assist the attenuation offered to the power supply ripple whilst requiring a trade-off to be calculated with the

recharge rate of the sampling capacitor in its power delivery role. Improved isolation between the circuitry considered to be insensitive and sensitive would aid the result.

4. The auto-tuned resonant filter has wider applications in such areas as automatically filtering RF interferers in radio circuitry, being placed on-board a mixed-signal system-on-chip such that any relatively noisy power supply intended for digital circuitry could be directly connected to the system, etc. There are many other possible applications and refinements that can this core technology can be used for. The technique is not limited to power supplies or power supply frequencies.

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Appendices

Appendix A

ADM1166 Power Supply Manager defined by the author in early stages of research.

ANALOG DEVICES

Super Sequencer with Margining Control and Nonvolatile Fault Recording

Data Sheet **ADM1166**

FEATURES

- Complete supervisory and sequencing solution for up to 10 supplies
- 16 event deep black box nonvolatile fault recording
- 10 supply fault detectors enable supervision of supplies to
  - <0.5% accuracy at all voltages at 25°C
  - <1.0% accuracy across all voltages and temperatures
- 5 selectable input attenuators allow supervision of supplies to 14.4 V on VH and 6 V on VP1 to VP4 (VPx)
- 5 dual-function inputs, VX1 to VX5 (VXx)
  - High impedance input to supply fault detector with thresholds between 0.573 V and 1.375 V
  - General-purpose logic input
- 10 programmable driver outputs, PDO1 to PDO10 (PDOx)
  - Open-collector with external pull-up
  - Push/pull output, driven to VDDCAP or VPx
  - Open collector with weak pull-up to VDDCAP or VPx
  - Internally charge-pumped high drive for use with external N-FET (PDO1 to PDO6 only)
- SE implements state machine control of PDO outputs
  - State changes conditional on input events
  - Enables complex control of boards
  - Power-up and power-down sequence control
  - Fault event handling
  - Interrupt generation on warnings
  - Watchdog function can be integrated in SE
  - Program software control of sequencing through SMBus
- Complete voltage-margining solution for 6 voltage rails
- 6 voltage output 8-bit DACs (0.300 V to 1.551 V) allow voltage adjustment via dc-to-dc converter trim/feedback node
- 12-bit ADC for readback of all supervised voltages
- 2 auxiliary (single-ended) ADC inputs
- Reference input (REFIN) has 2 input options
  - Driven directly from 2.048 V (±0.25%) REFOUT pin
  - More accurate external reference for improved ADC performance
- Device powered by the highest of VPx, VH for improved redundancy
- User EEPROM: 256 bytes
- Industry-standard 2-wire bus interface (SMBus)
- Guaranteed PDO low with VH, VPx = 1.2 V
- Available in 40-lead, 6 mm × 6 mm LFCSP and 48-lead, 7 mm × 7 mm TQFP packages

FUNCTIONAL BLOCK DIAGRAM

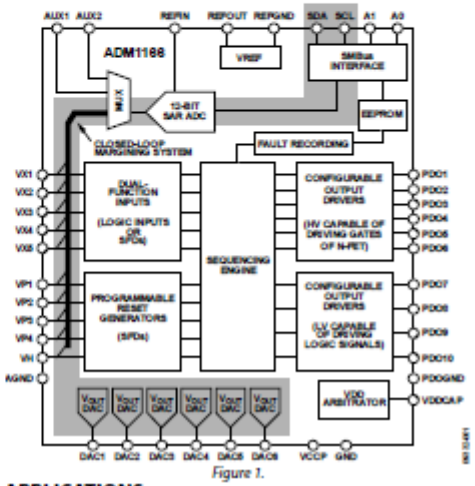

Figure 1.

APPLICATIONS

- Central office systems
- Servers/routers
- Multivoltage system line cards
- DSP/FPGA supply sequencing
- In-circuit testing of margined supplies

GENERAL DESCRIPTION

The ADM1166 Super Sequencer® is a configurable supervisory/sequencing device that offers a single-chip solution for supply monitoring and sequencing in multiple-supply systems. In addition to these functions, the ADM1166 integrates a 12-bit ADC and six 8-bit voltage output DACs. These circuits can be used to implement a closed-loop margining system that enables supply adjustment by altering either the feedback node or reference of a dc-to-dc converter using the DAC outputs.

Supply margining can be performed with a minimum of external components. The margining loop can be used for in-circuit testing of a board during production (for example, to verify board functionality at −5% of nominal supplies), or it can be used dynamically to accurately control the output voltage of a dc-to-dc converter.

For more information about the ADM1166 register map, refer to the AN-698 Application Note.

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Tel: 781.329.4700
Technical Support www.analog.com

Appendix B

ADM7150 Linear Regulator designed as a direct outcome of this work.

ANALOG DEVICES

800 mA Ultralow Noise, High PSRR, RF Linear Regulator

Data Sheet **ADM7150**

FEATURES

- Input voltage range: 4.5 V to 16 V
- Maximum output current: 800 mA
- Low noise
  - 1.0 µV rms total integrated noise from 100 Hz to 100 kHz
  - 1.6 µV rms total integrated noise from 10 Hz to 100 kHz
- Noise spectral density: 1.7 nV/√Hz typical from 10 kHz to 1 MHz
- Power supply rejection ratio (PSRR) at 400 mA load
  - >90 dB from 1 kHz to 100 kHz, V_{OUT} = 5 V
  - >60 dB at 1 MHz, V_{OUT} = 5 V
- Dropout voltage: 0.6 V at V_{OUT} = 5 V, 800 mA load
- Initial voltage accuracy: ±1%
- Voltage accuracy over line, load and temperature: ±2%
- Quiescent current (I_{GND}): 4.3 mA at no load
- Low shutdown current: 0.1 µA
- Stable with a 10 µF ceramic output capacitor
- Fixed output voltage options: 1.8 V, 2.8 V, 3.0 V, 3.3 V, 4.5 V, 4.8 V, and 5.0 V (16 outputs between 1.5 V and 5.0 V are available)
- Exposed pad 8-lead LFCSP and 8-lead SOIC packages

APPLICATIONS

- Regulated power noise sensitive applications
  - RF mixers, phase-locked loops (PLLs), voltage-controlled oscillators (VCOs), and PLLs with integrated VCOs
- Communications and infrastructure
- Cable digital-to-analog converter (DAC) drivers
- Backhaul and microwave links

TYPICAL APPLICATION CIRCUIT

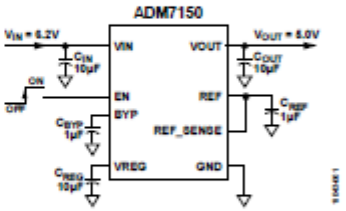

Figure 1. 5 V Output Circuit

GENERAL DESCRIPTION

The ADM7150 is a low dropout (LDO) linear regulator that operates from 4.5 V to 16 V and provides up to 800 mA of output current. Using an advanced proprietary architecture, it provides high power supply rejection (>90 dB from 1 kHz to 1 MHz), ultralow output noise (<1.7 nV/√Hz), and achieves excellent line and load transient response with a 10 µF ceramic output capacitor.

The ADM7150 is available in 1.8 V, 2.8 V, 3.0 V, 3.3 V, 4.5 V, 4.8 V, and 5.0 V fixed outputs. In addition, 16 fixed output voltages between 1.5 V and 5.0 V are available upon request.

The ADM7150 regulator typical output noise is 1.0 µV rms from 100 Hz to 100 kHz for fixed output voltage options, and the noise spectral density is 1.7 nV/√Hz from 10 kHz to 1 MHz.

The ADM7150 is available in 8-lead, 3 mm × 3 mm LFCSP and 8-lead SOIC packages, making it not only a very compact solution but also providing excellent thermal performance for applications requiring up to 800 mA of output current in a small, low profile footprint. See the ADM7151 adjustable LDO to generate additional output voltages.

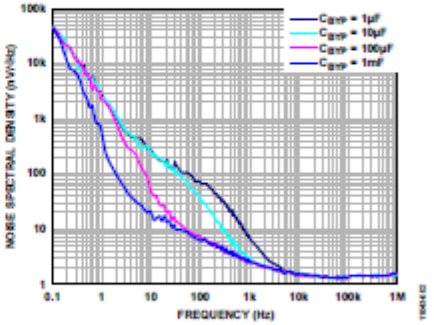

Figure 2. Noise Spectral Density (NSD) vs. Frequency for Various Cer

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Appendix C

Patent granted on use of resonance to post filter a switching regulator

US008885376B2

(12) **United States Patent**
Meehan et al.

(10) **Patent No.: US 8,885,376 B2**
(45) **Date of Patent: Nov. 11, 2014**

(54) **SWITCHING REGULATOR WITH INTEGRATED RESONANT CIRCUIT FOR RIPPLE FILTERING**

(75) Inventors: **Patrick J. Meehan**, Pallaskenry (IE); **Thomas Conway**, Castletroy (IE); **Aldrick Limjoco**, Dasmarinas (PH); **Donal G. O'Sullivan**, Ardnacrusha (IE)

(73) Assignee: **Analog Devices, Inc.**, Norwood, MA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 258 days.

(21) Appl. No.: **13/484,636**

(22) Filed: **May 31, 2012**

(65) **Prior Publication Data**

US 2013/0320943 A1 Dec. 5, 2013

(51) **Int. Cl.**
H02M 1/14 (2006.01)
G05F 1/10 (2006.01)

(52) **U.S. Cl.**
CPC ***G05F 1/10*** (2013.01)
USPC **363/147**; 333/184; 327/290

(58) **Field of Classification Search**
CPC H02M 1/14; H02M 1/143; H02M 1/15
USPC 363/147; 323/290; 327/556, 290; 307/105; 333/181, 184
See application file for complete search history.

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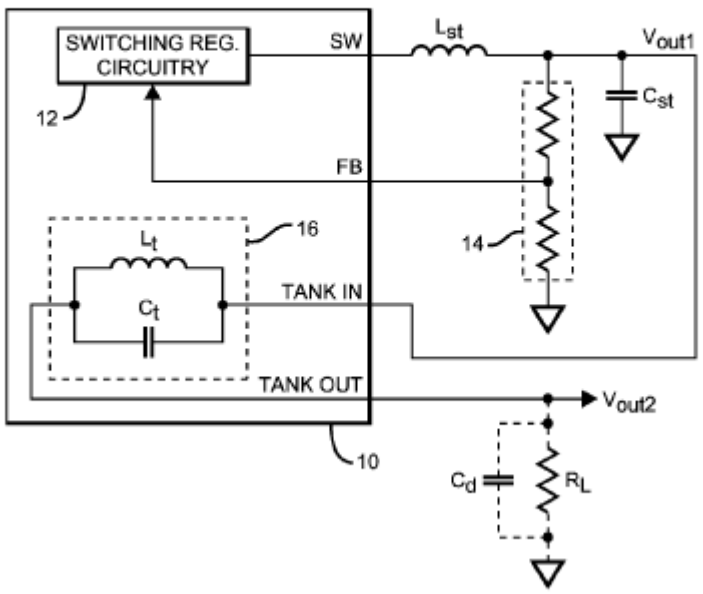
Primary Examiner — Harry Behm
(74) *Attorney, Agent, or Firm* — Schwegman Lundberg & Woessner, P.A.

(57) **ABSTRACT**

A switching regulator IC contains both switching regulator circuitry and an inductor and a capacitor connected in parallel to form a resonant circuit having an associated notch filter frequency response arranged such that, when connected to receive the regulated output voltage, the resonant circuit attenuates the ripple component. This is accomplished by matching the resonant notch to the ripple's fundamental frequency, either manually or automatically. In addition, the resonant circuit's inductor and capacitor can act in concert with decoupling capacitors coupled to the load to form a low pass filter which attenuates harmonics of the ripple's fundamental frequency.

23 Claims, 4 Drawing Sheets



Appendix D

Patent granted on use of supply-sampling.

(12) **United States Patent**
Meehan et al.

(10) **Patent No.: US 8,975,953 B2**
(45) **Date of Patent: Mar. 10, 2015**

(54) **METHOD OF IMPROVING NOISE IMMUNITY IN A SIGNAL PROCESSING APPARATUS, AND A SIGNAL PROCESSING APPARATUS HAVING IMPROVED NOISE IMMUNITY**

(71) Applicant: **Analog Devices Technology**, Hamilton (BM)

(72) Inventors: **Patrick J. Meehan**, Limerick (IE); **Mark T. Kelly**, Limerick (IE); **Christopher Peter Hurrell**, Berkshire (GB); **Thomas Anthony Conway**, Limerick (IE); **Donal O'Sullivan**, Co. Clare (IE); **Michael Hennessy**, Limerick (IE); **William Hunt**, Limerick (IE)

(73) Assignee: **Analog Devices Global**, Hamilton (BM)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **13/793,543**

(22) Filed: **Mar. 11, 2013**

(65) **Prior Publication Data**

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(51) **Int. Cl.**
H03K 3/01 (2006.01)
H03K 17/00 (2006.01)

(52) **U.S. Cl.**
CPC ***H03K 17/00*** (2013.01)
USPC **327/534**; 327/545

(58) **Field of Classification Search**
CPC G05F 1/467
USPC 327/530, 534, 538, 543, 545
See application file for complete search history.

(56) **References Cited**

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Primary Examiner — Jeffrey Zweizig
(74) *Attorney, Agent, or Firm* — Patent Capital Group

(57) **ABSTRACT**

A signal processing apparatus that includes a circuit in which a signal processing function is performed during a first time period, the signal processing apparatus including or being associated with a switch or a filter in a power supply to the signal processing apparatus so as to disconnect the signal processing apparatus from the power supply or to filter the power supply during a second time period that is coincident with at least part of the first time period.

17 Claims, 5 Drawing Sheets